

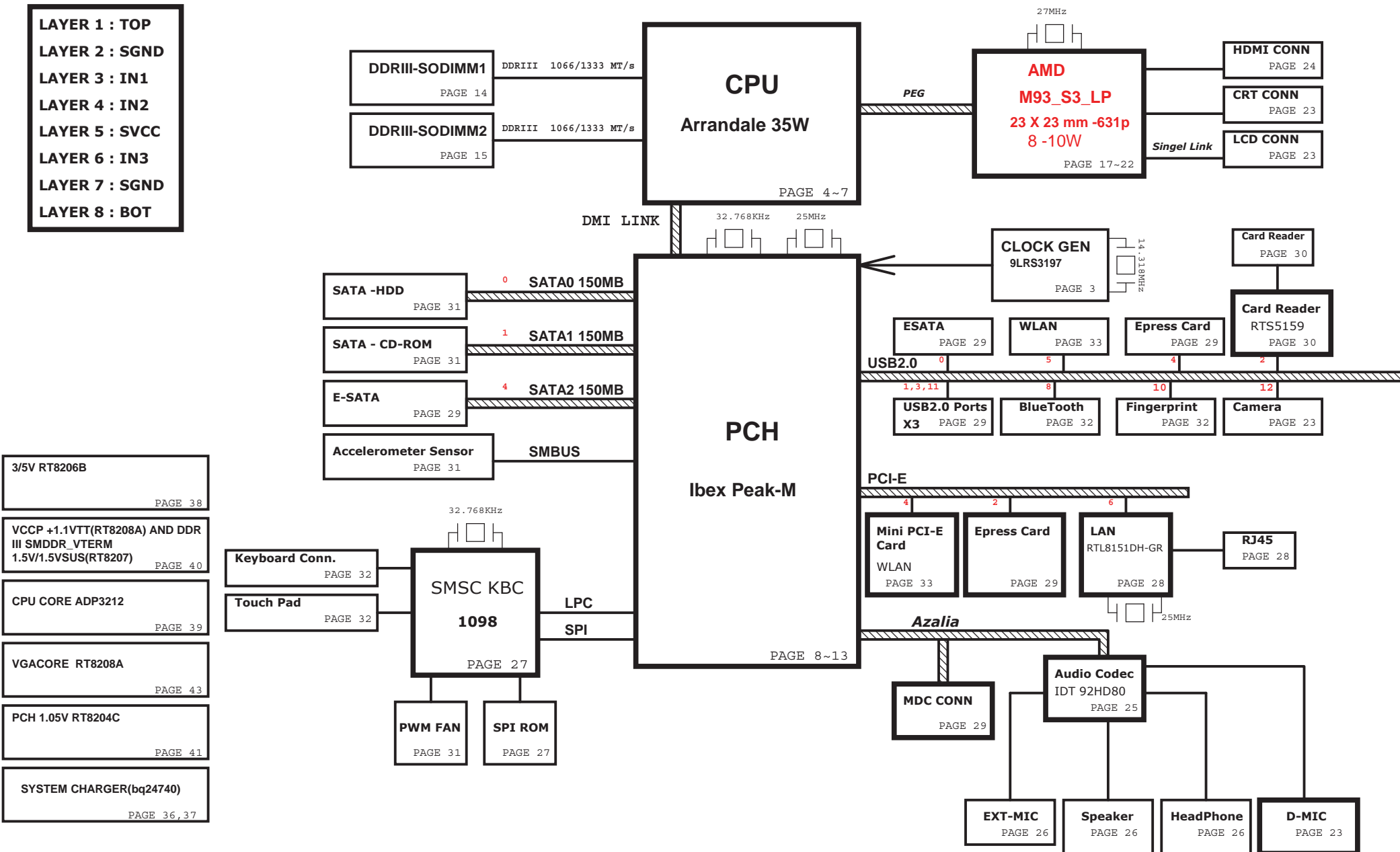
PCB STACK UP

8L Dis.

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND
- LAYER 8 : BOT

Hamilton 1.0 (SX6-DIS) BLOCK DIAGRAM

01



<http://laptop-motherboard-schematic.blogspot.com/>

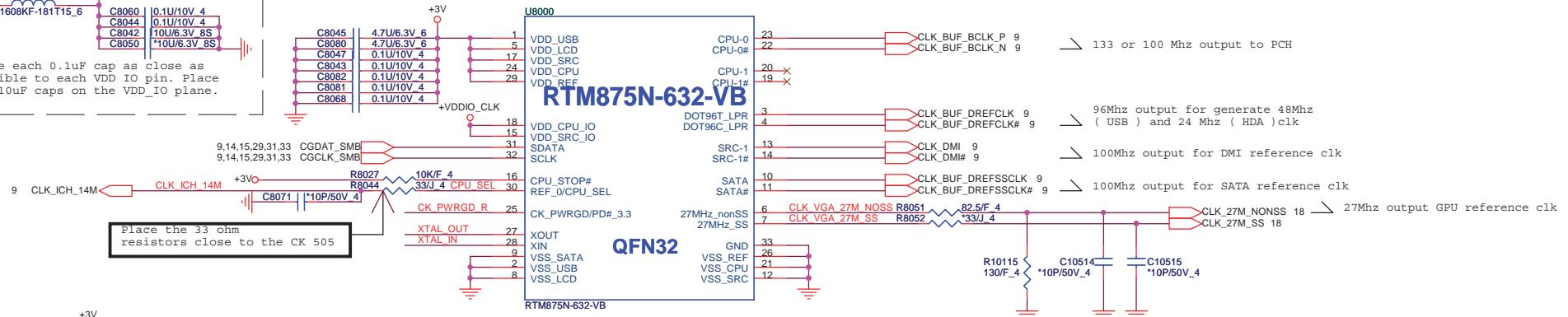
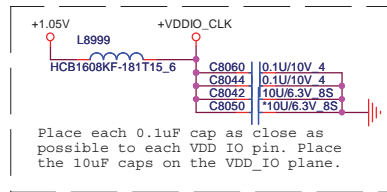
power State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98 (Write) / 0x99 (Read)	G-SENSOR 0x3A (Write) / 0x3B (Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA2	SMSC 1098	GPU thermal sensor
SMBCLK SMBDATA	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_CLK_ME1 SMB_DAT_ME1	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1098	Y	X	X	X	X	X	X	X

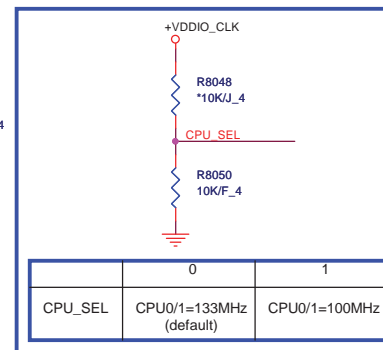
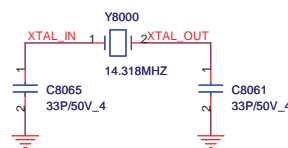
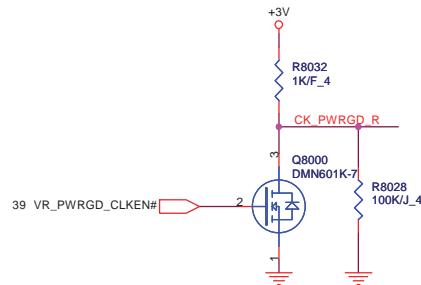


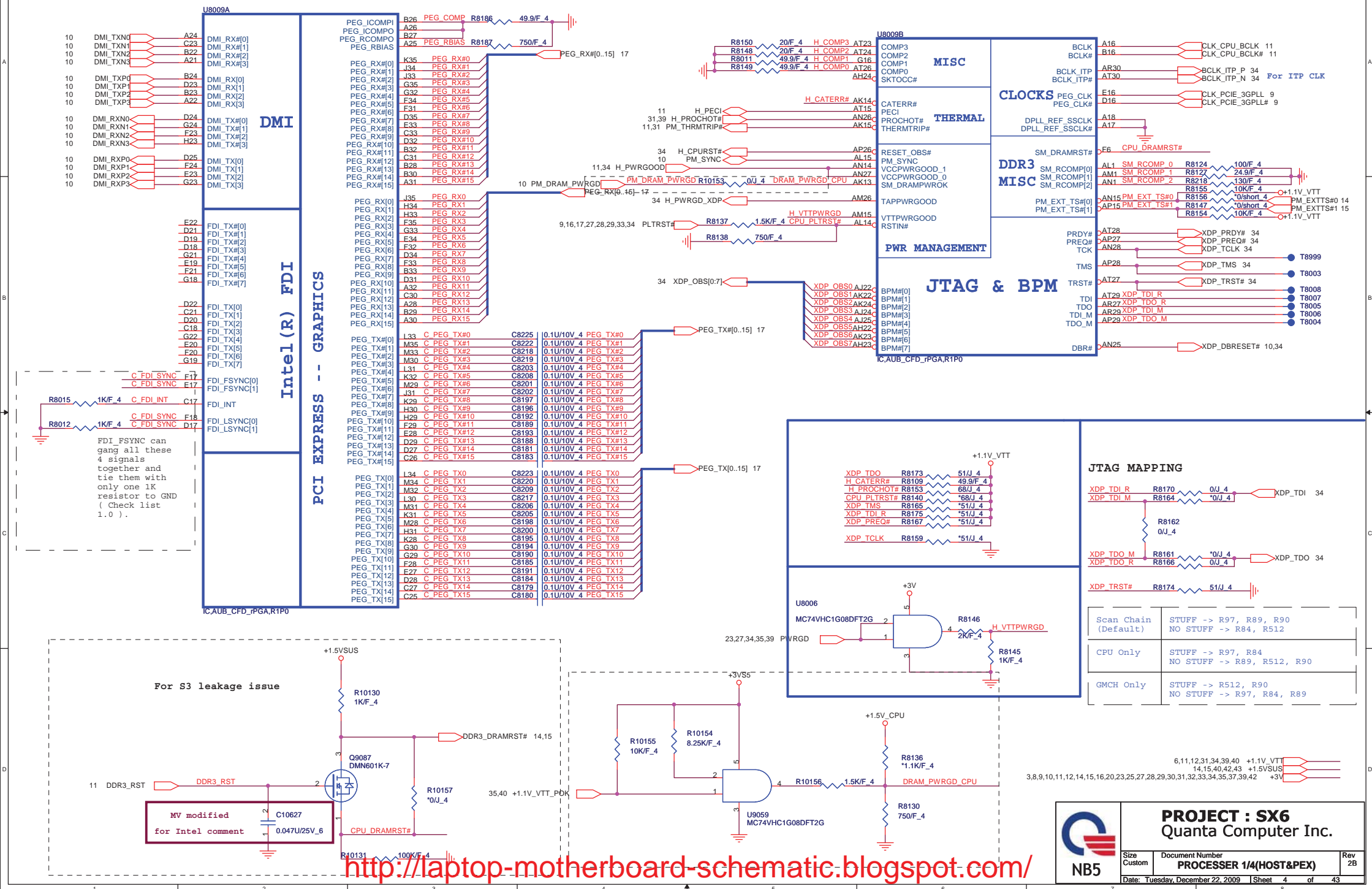
PROJECT : SX6
Quanta Computer Inc.

Size Custom	Document Number power rails	Rev 2B
Date: Tuesday, December 15, 2009 Sheet 2 of 43		

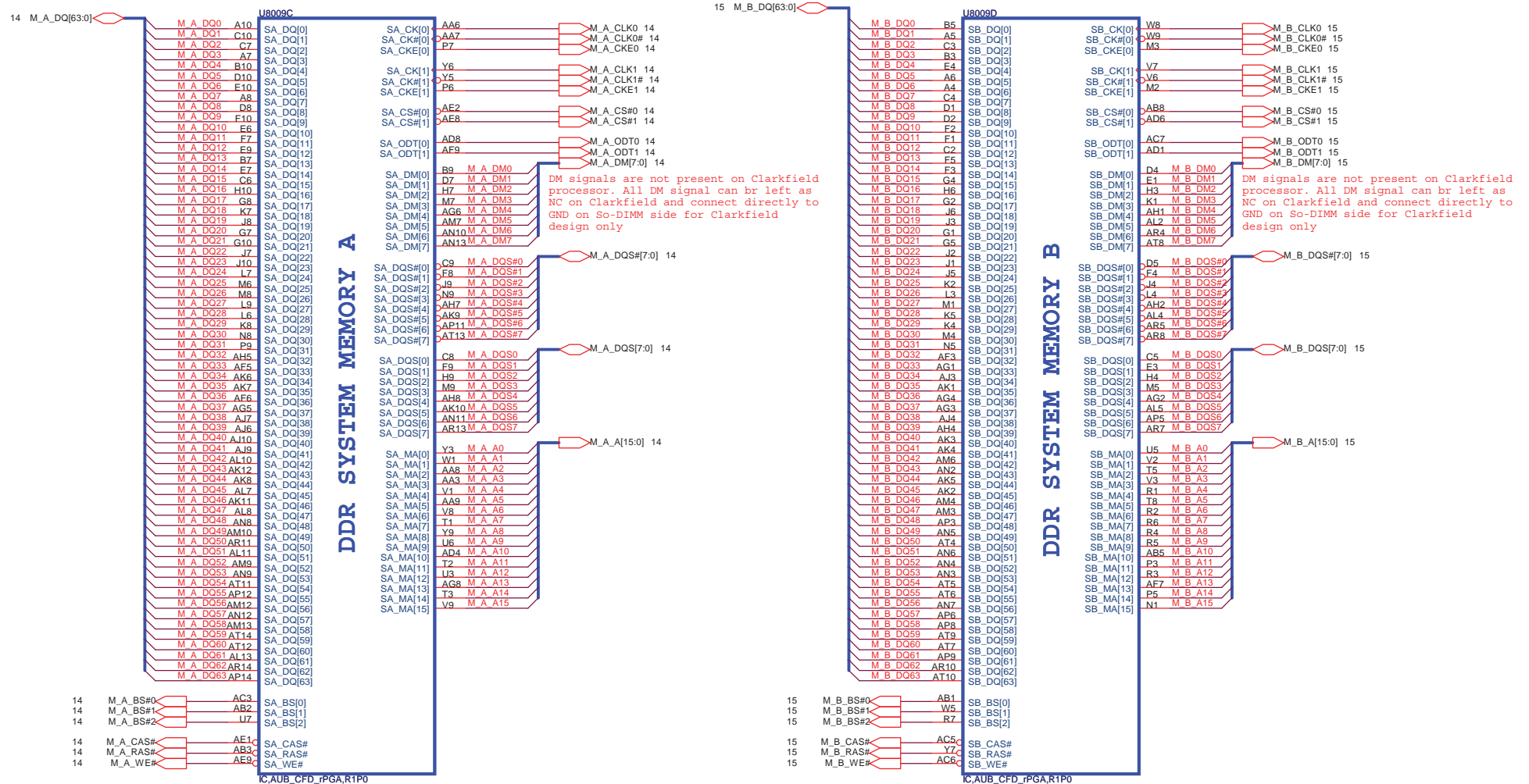


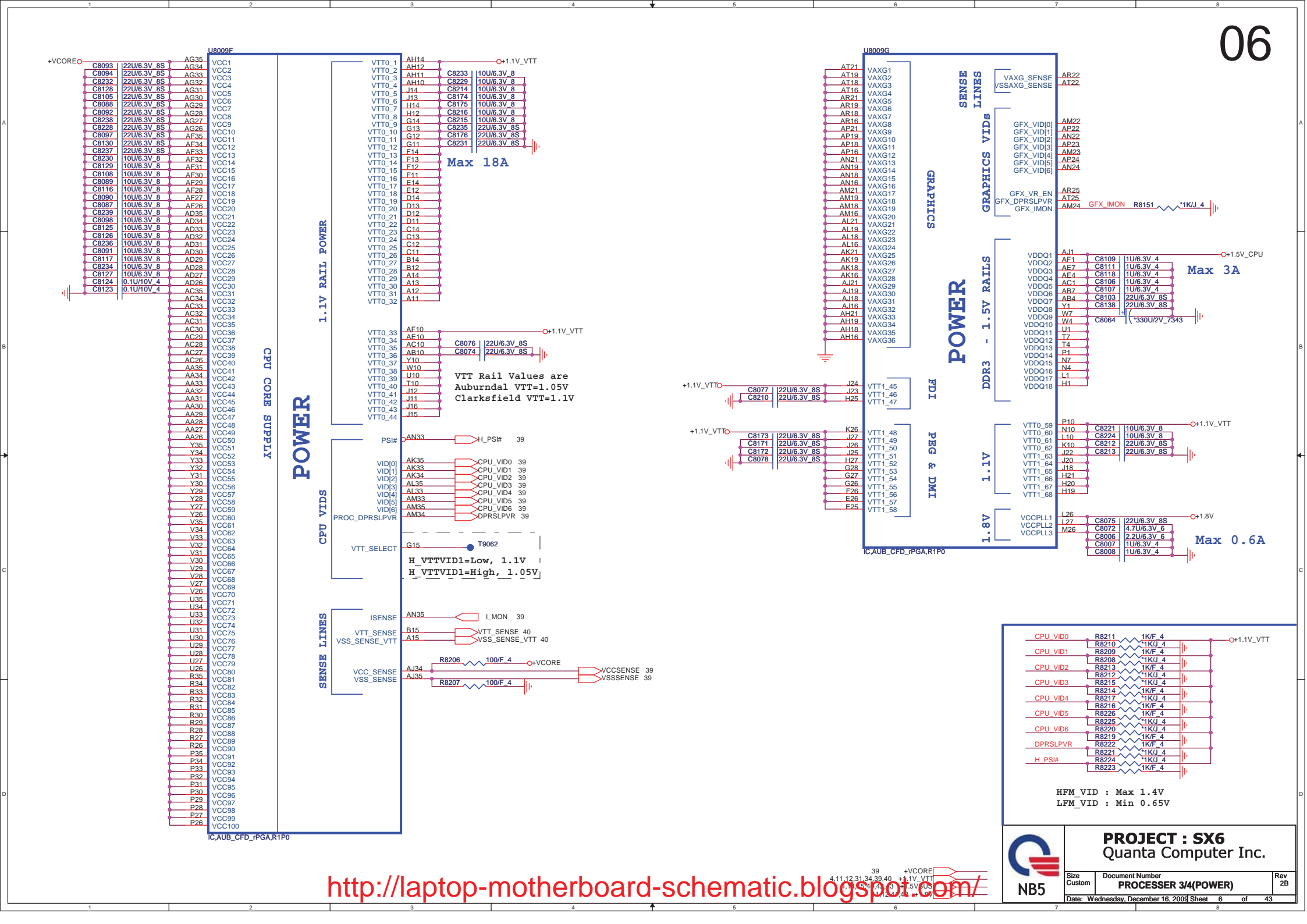
AL000875002IC OTHER(32P) RTM875N-632-VB-GRT(QFN)Realtek
AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)Silego





AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

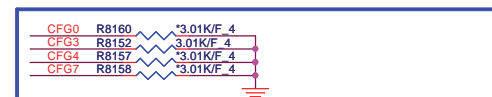
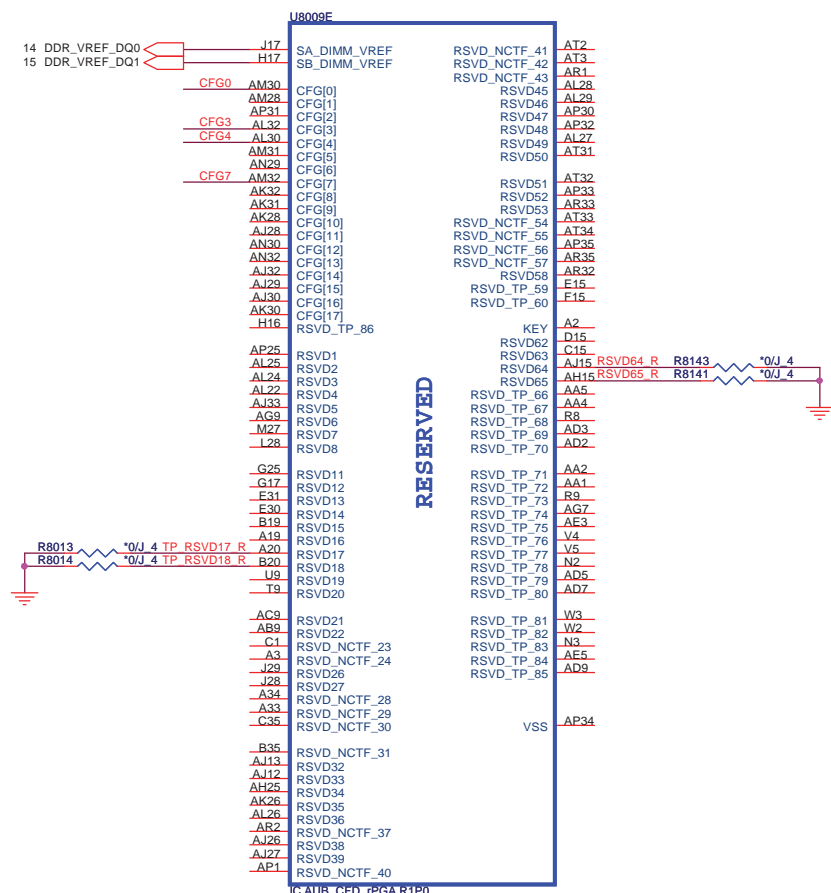
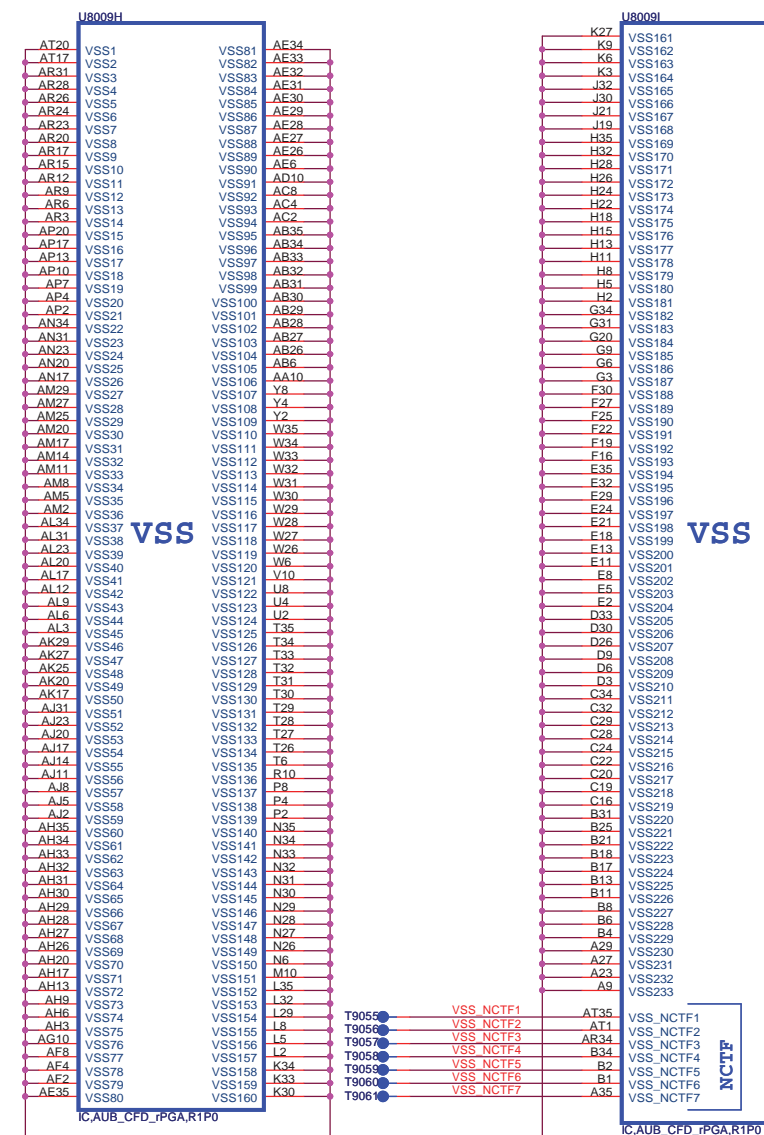




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

07



CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

PROJECT : SX6
Quanta Computer Inc.

Size Custom	Document Number PROCESSOR 4/4(GND)	Rev 2B
Date: Tuesday, December 15, 2009 Sheet 7 of 43		

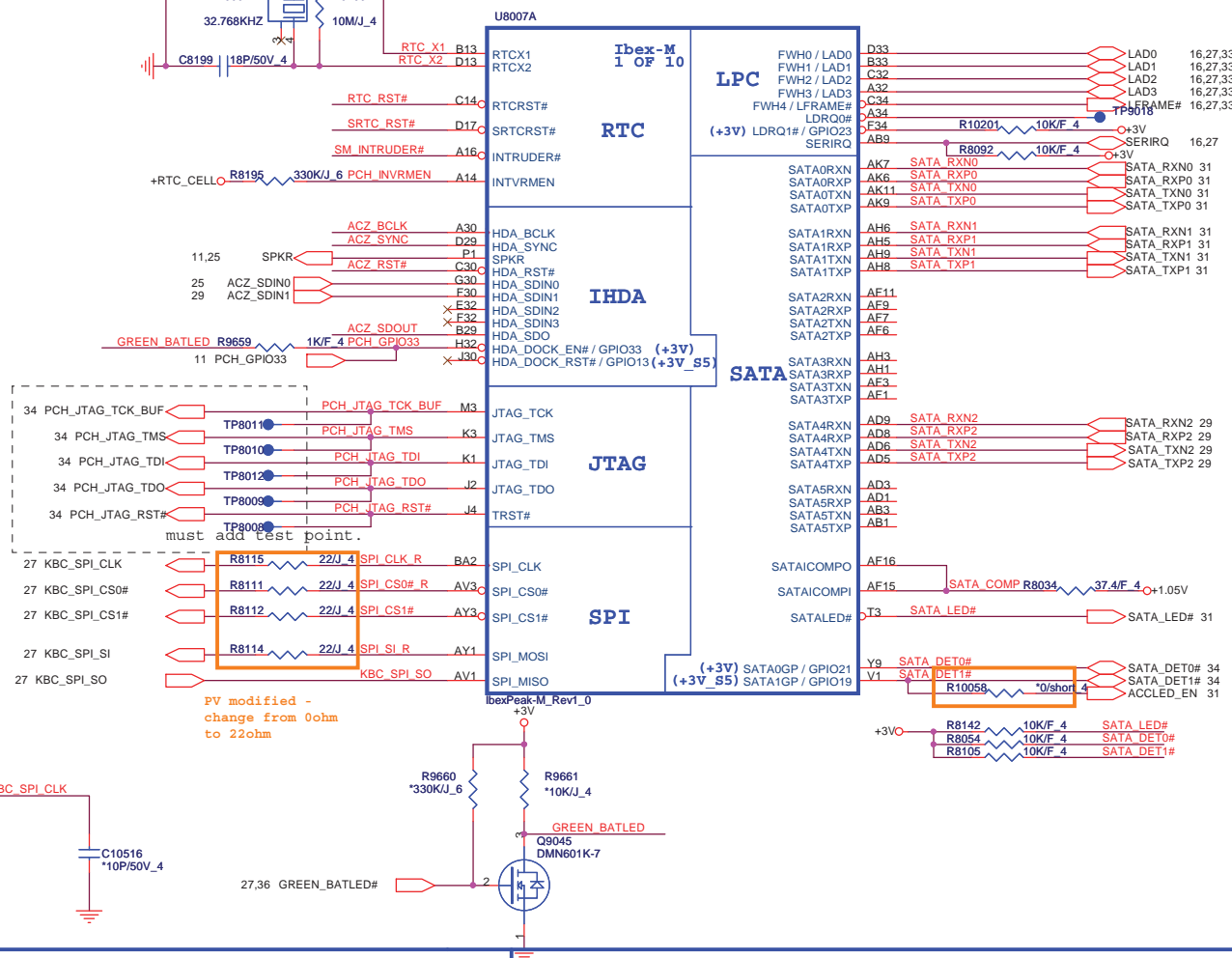
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

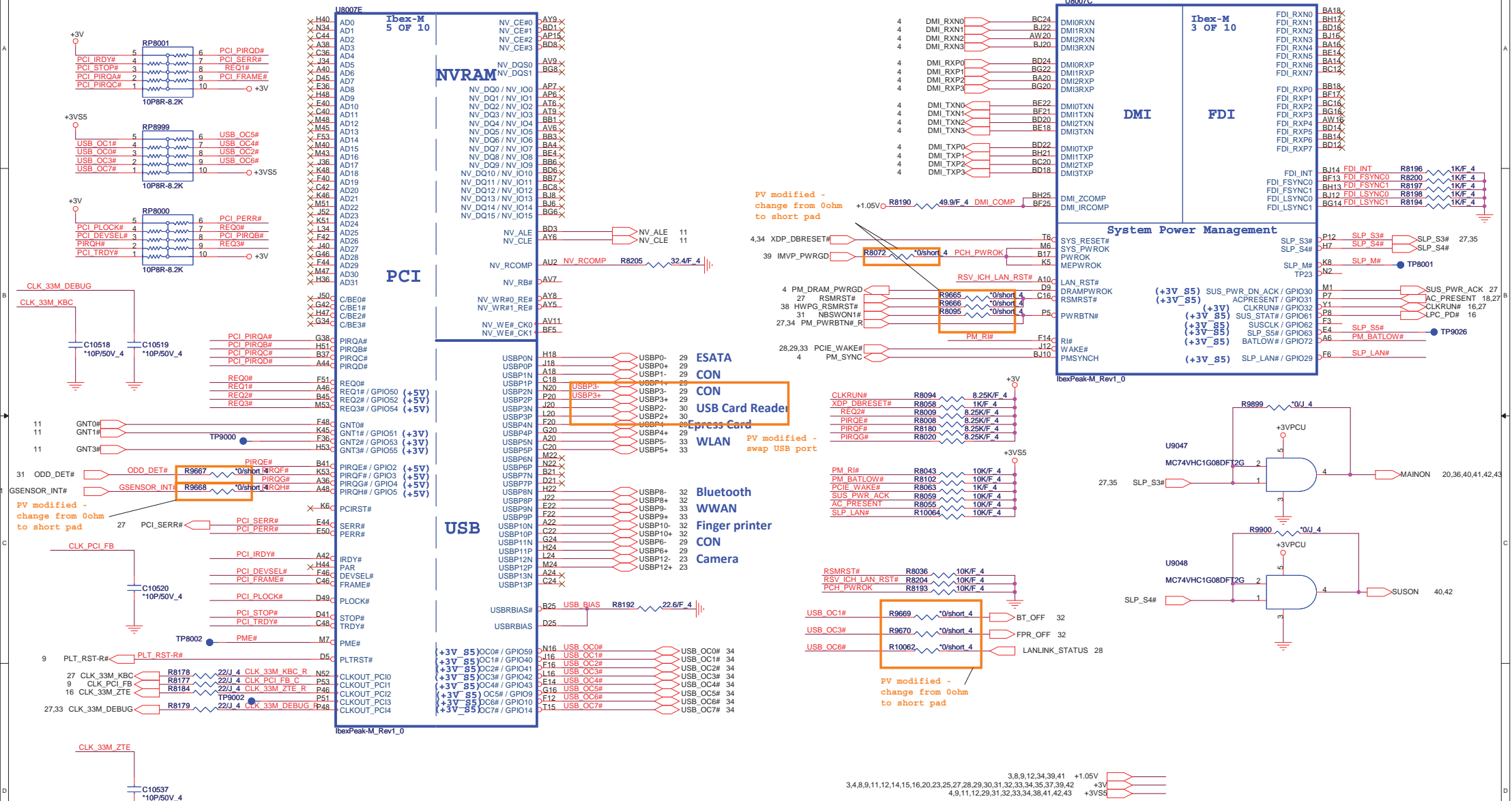


09



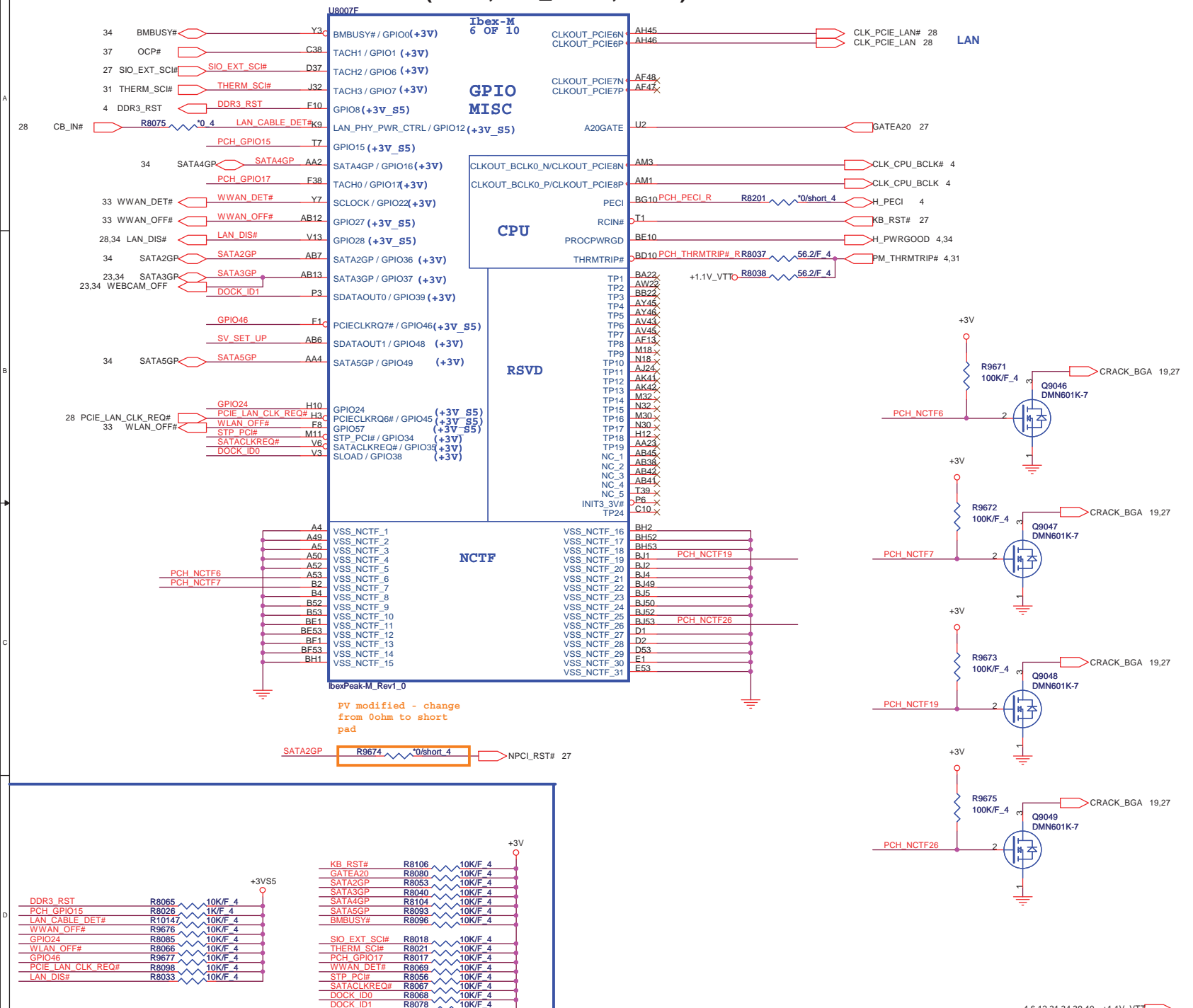
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

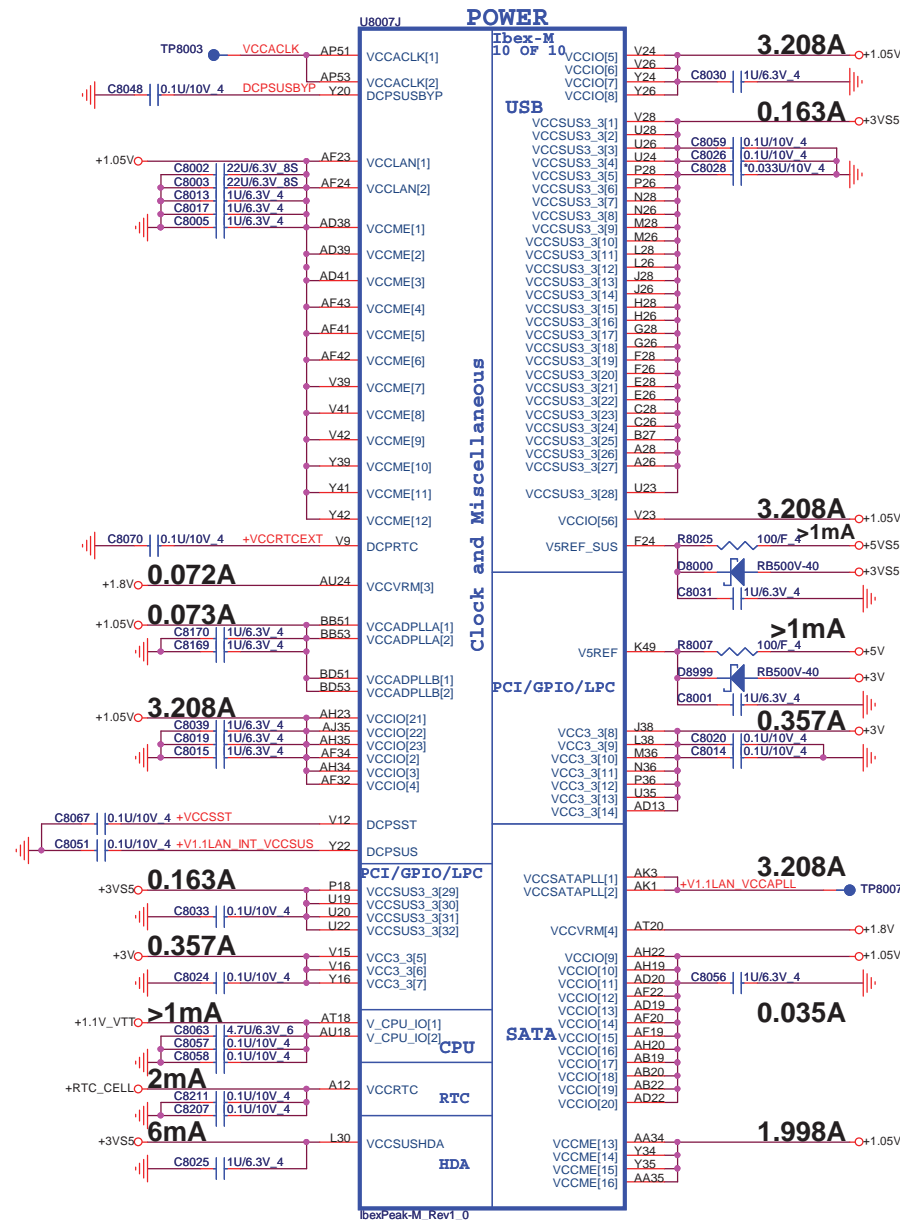
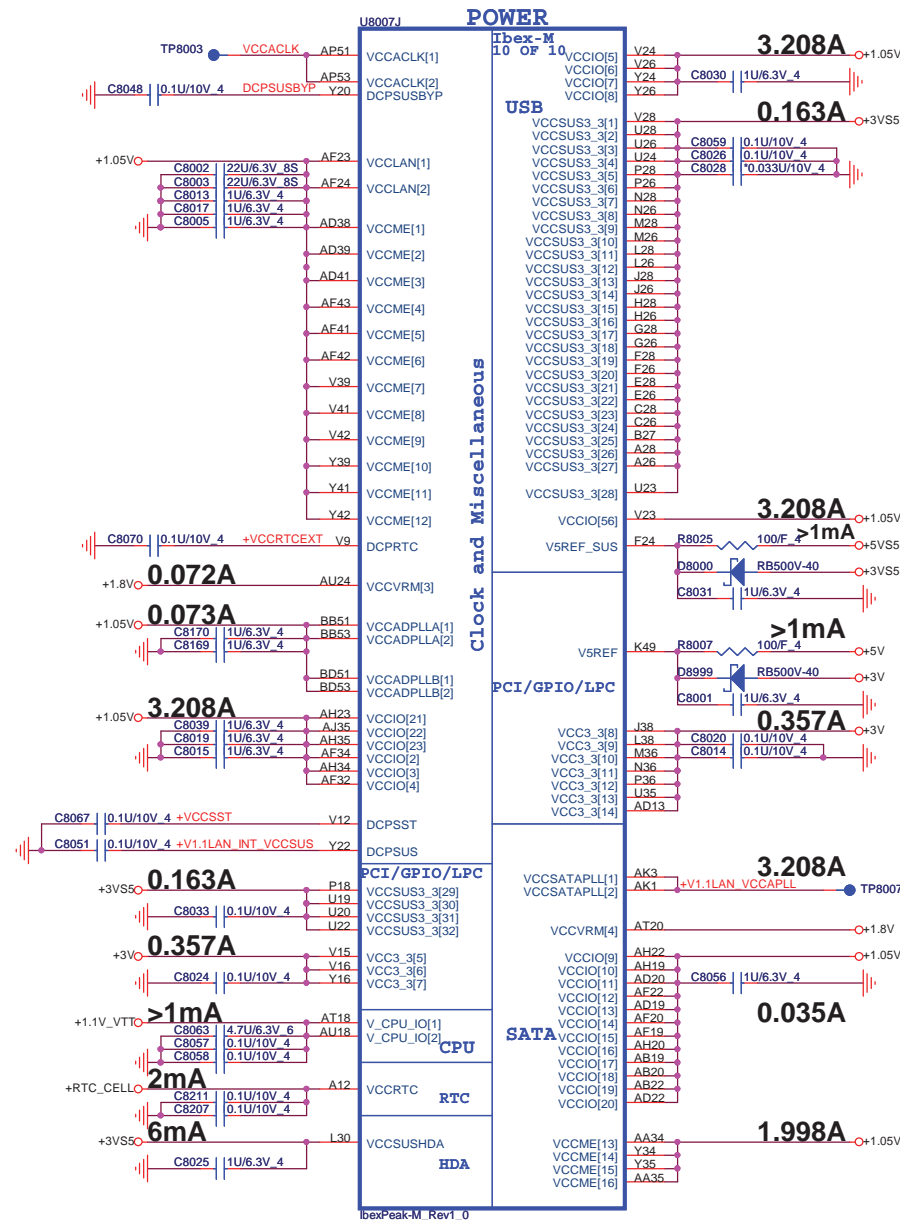
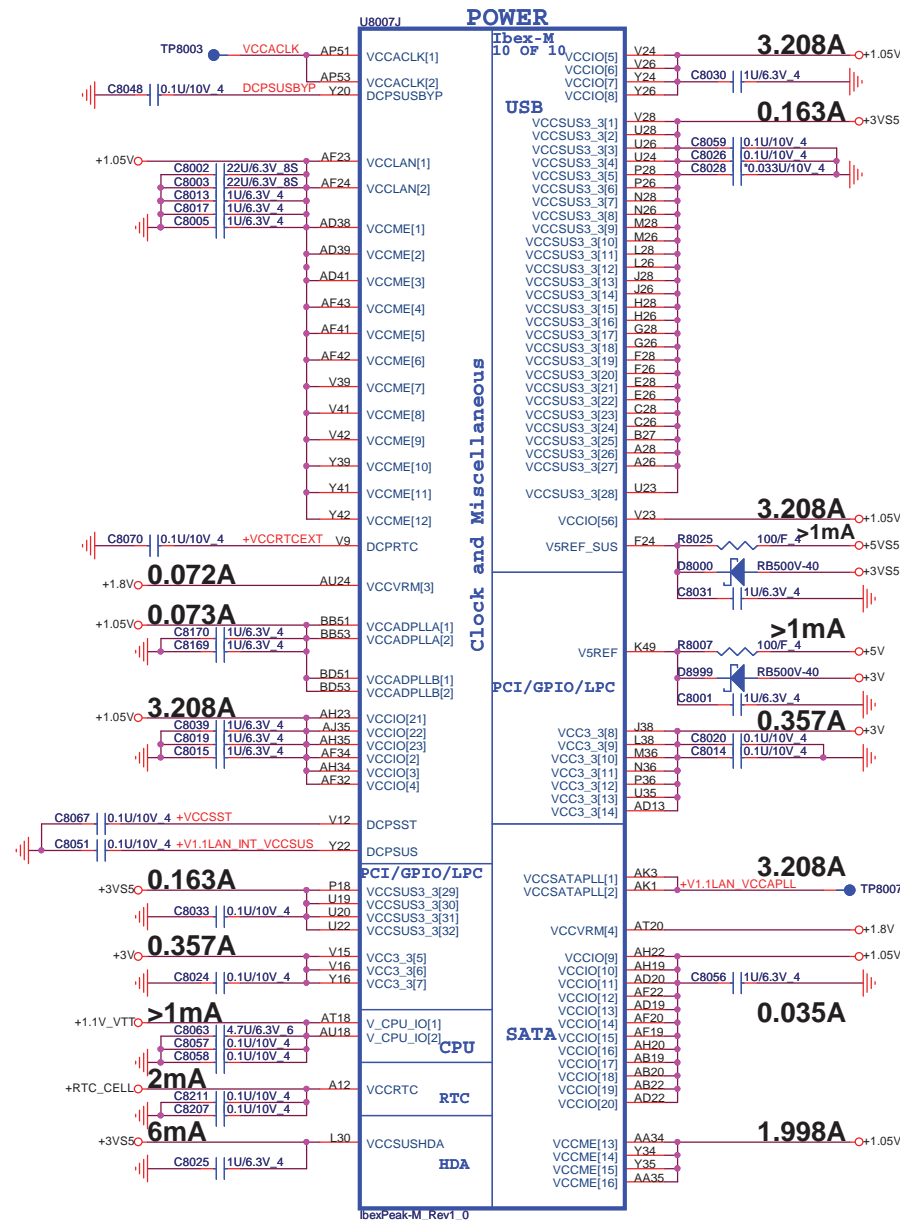


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

11

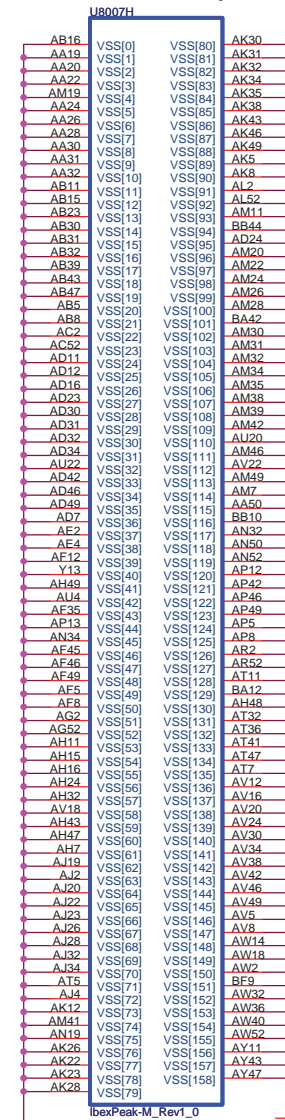
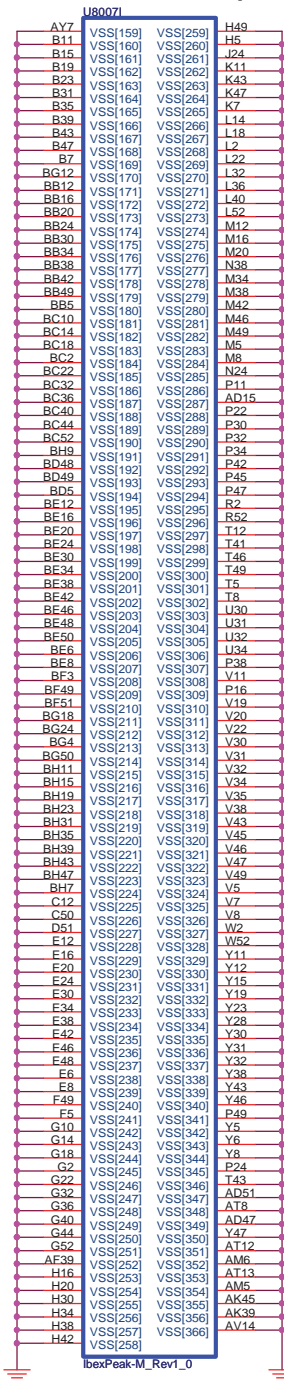


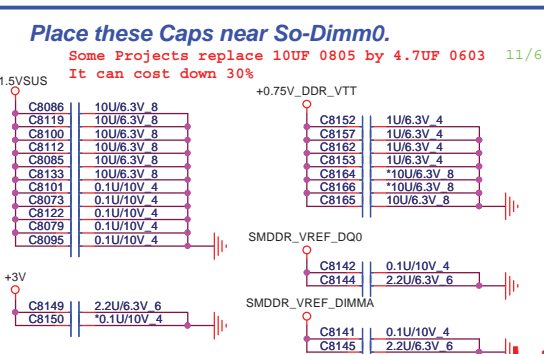
<http://laptop-motherboard-schematic.blogspot.com/>



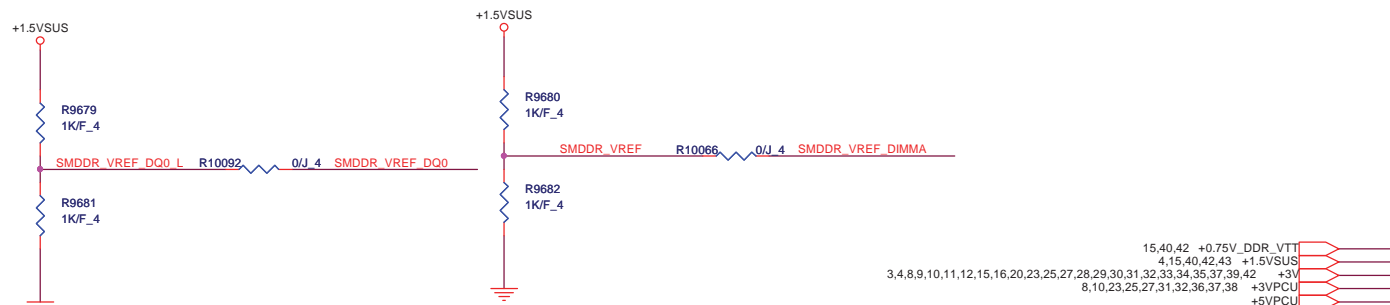
IBEX PEAK-M (GND)

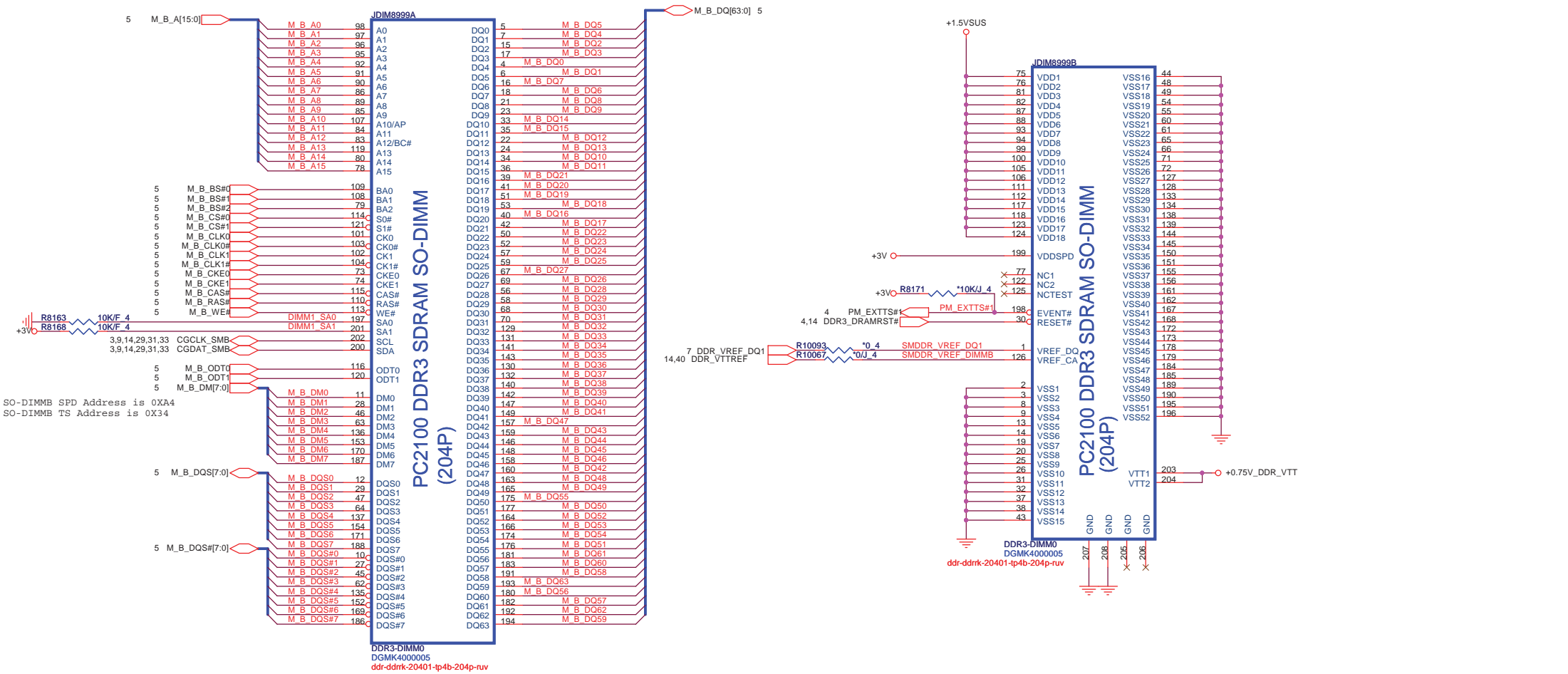
IBEX PEAK-M (GND)





<http://laptop-motherboard-schematic.blogspot.com/>





Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%

+1.5VSUS

C8083 10U/6.3V 8
 C8099 10U/6.3V 8
 C8115 10U/6.3V 8
 C8134 10U/6.3V 8
 C8053 10U/6.3V 8
 C8120 10U/6.3V 8
 C8110 0.1U/10V 4
 C8055 0.1U/10V 4
 C8121 0.1U/10V 4
 C8096 0.1U/10V 4
 C8084 0.1U/10V 4

+0.75V_DDR_VTT

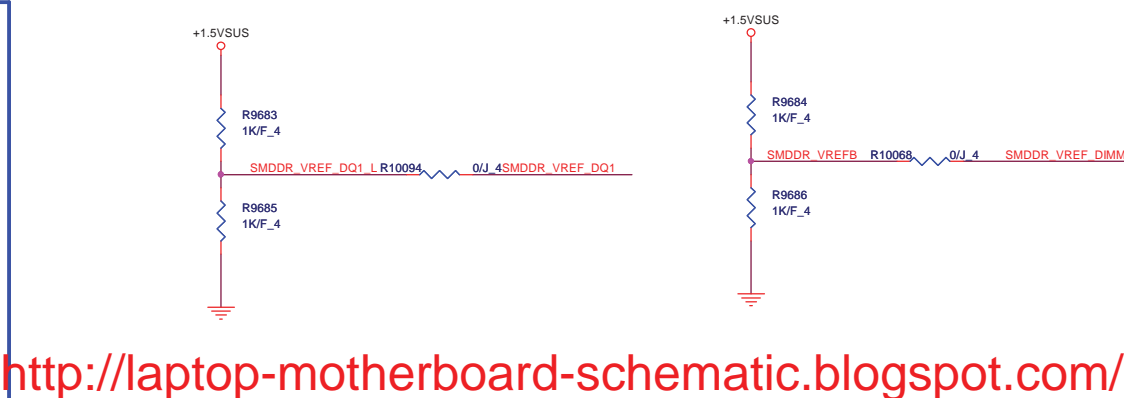
C8158 1U/6.3V 4
 C8159 1U/6.3V 4
 C8160 1U/6.3V 4
 C8161 1U/6.3V 4
 C8162 10U/6.3V 8
 C8156 10U/6.3V 8
 C8157 10U/6.3V 8

SMDDR_VREF_DIMMB

C8132 0.1U/10V 4
 C8131 2.2U/6.3V 6

SMDDR_VREF_DQ1

C8137 0.1U/10V 4
 C8135 2.2U/6.3V 6



14,40,42 +0.75V_DDR_VTT
 4,14,40,42,43 +1.5VSUS
 3,4,8,9,10,11,12,14,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
 8,10,23,25,27,31,32,36,37,38 +5VPCU



MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Samsung E-die Hynix Orion-die	64*16-800MHZ 64*16-800MHZ	K4W101646B-NC12 R5TQ1063BFR-12C	AKD5LGGT503 AKD5LZGTW01

I.MEMID 0: ODM, 0:Quanta 1:Wistron
 II.MEMID 1: Vram size, 0:512MB, 1:1GB
 III.MEMID 2: Vram vender, 0:samsung, 1:hynix.

Hynix 512M	上件	不上件
0100	R9919	R9921, R9920, R9918

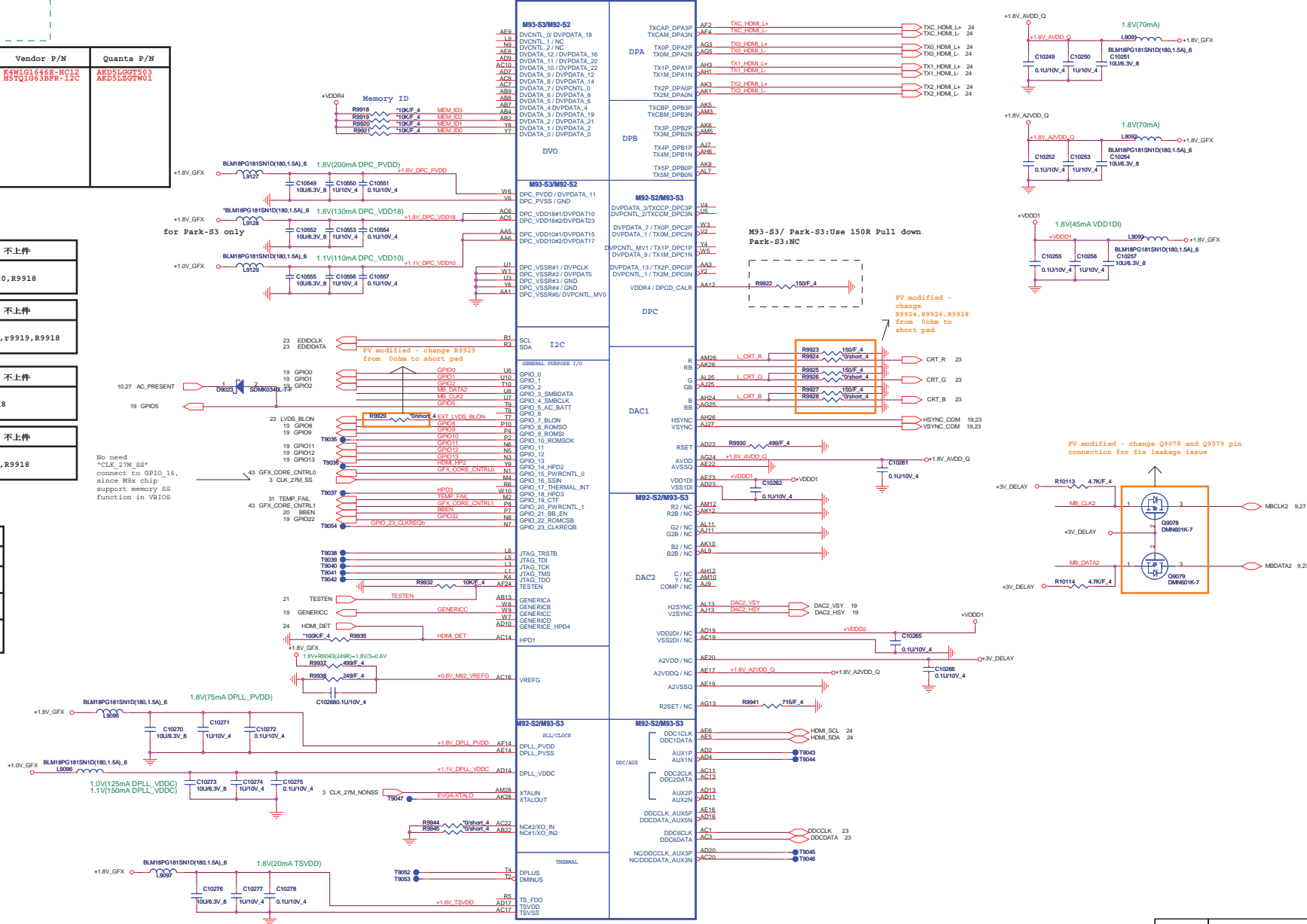
Samsung 512M	上件	不上件
0000	NA	R9921, R9920, R9919, R9918

Hynix 1G	上件	不上件
0110	R9919, R9920	R9921, R9918

Samsung 1G	上件	不上件
0010	R9920	R9921, R9919, R9918

PWRCNTL1	PWRCNTL0	V-CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

BBEN	BBP
L 0	V-CORE
H 1	+1.8V

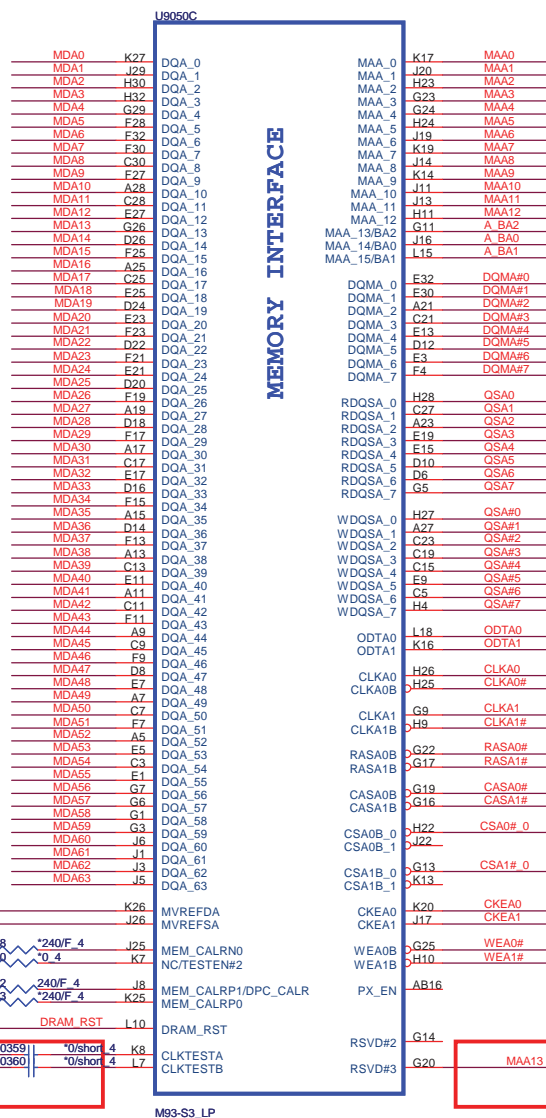
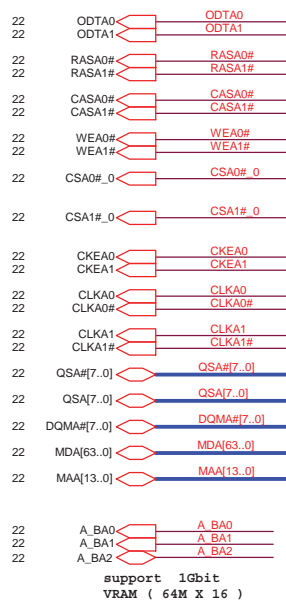




Memory Aperture size

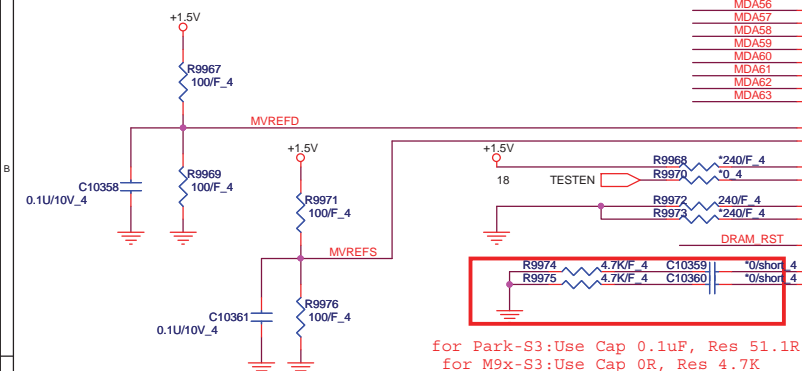
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.





MEMORY INTERFACE

for Park-S3:Use only
for M9x-S3: no support



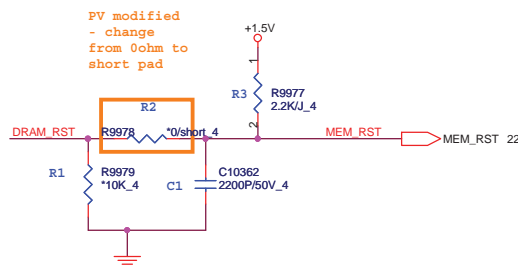
for Park-S3:Use Cap 0.1uF, Res 51.1R
for M9x-S3:Use Cap 0R, Res 4.7K

	M9x-S2/S3	Park-S3
MEM_CALRN0 (J25)	NC	240R
MEM_CALRP0 (K25)	NC	0R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	680R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

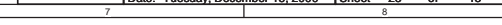
2.2nF:CH22206KB16
68pF:CH06806JB01

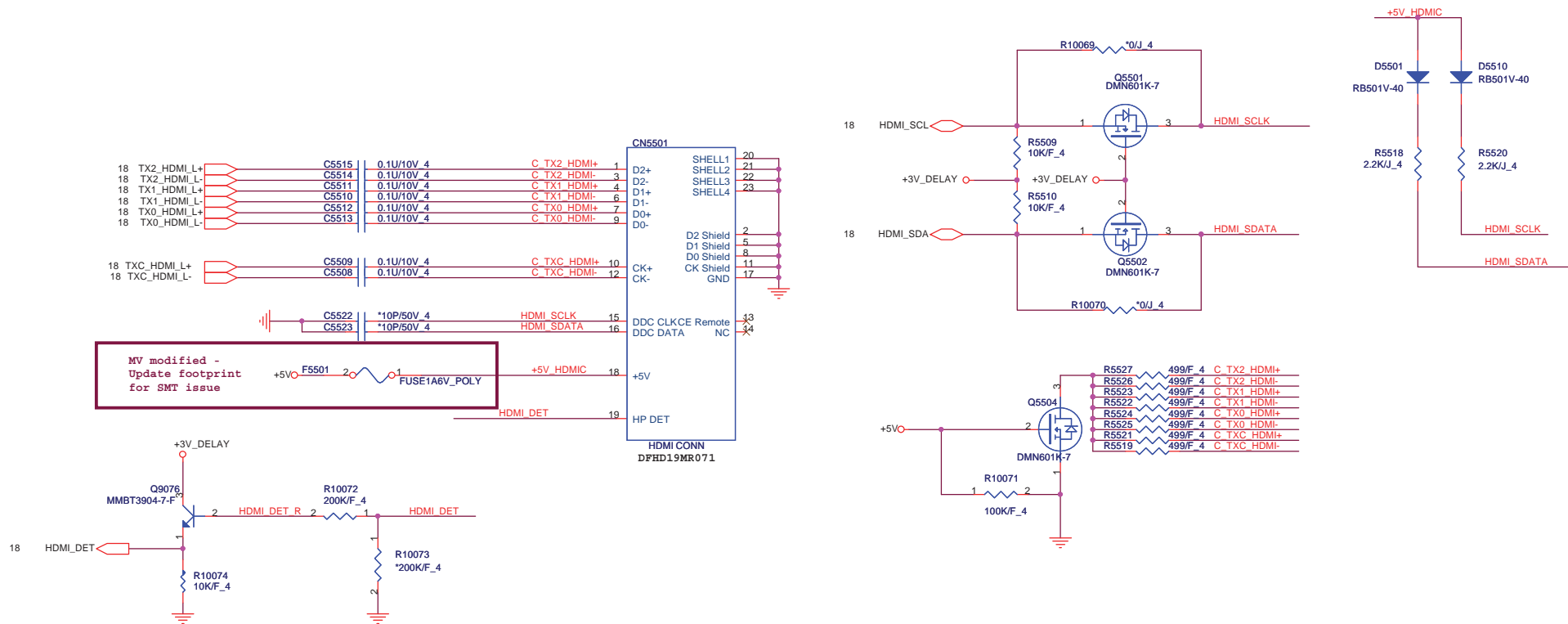


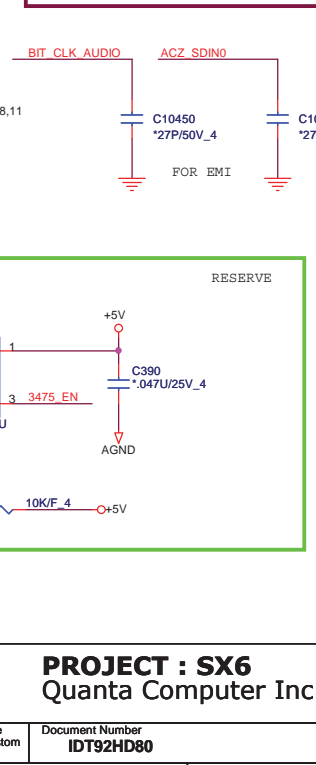
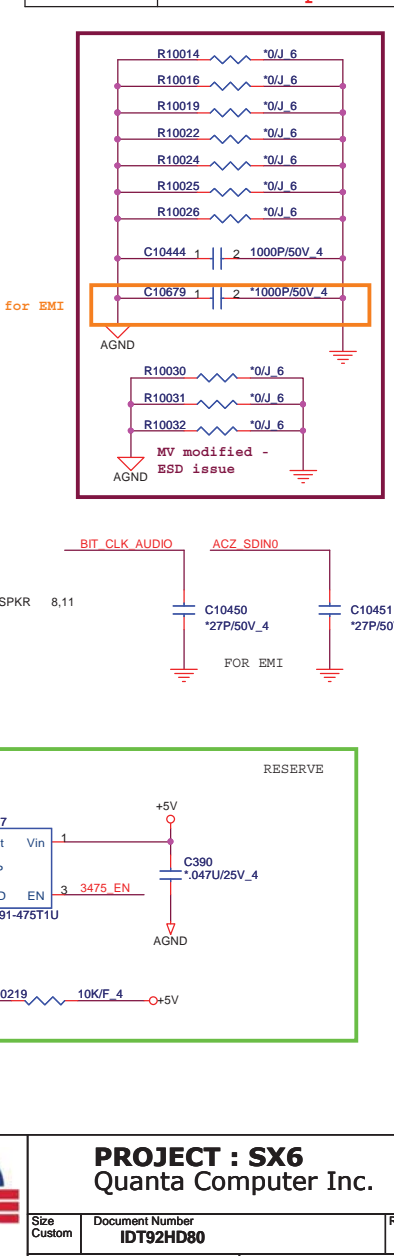
PROJECT : SX6
Quanta Computer Inc.

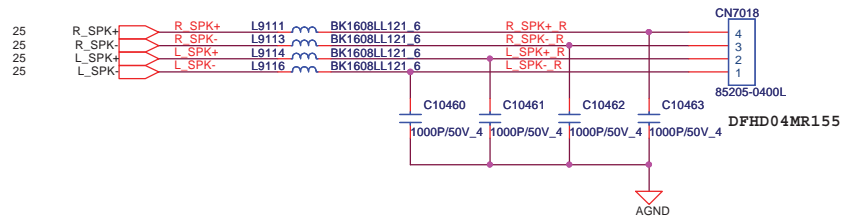
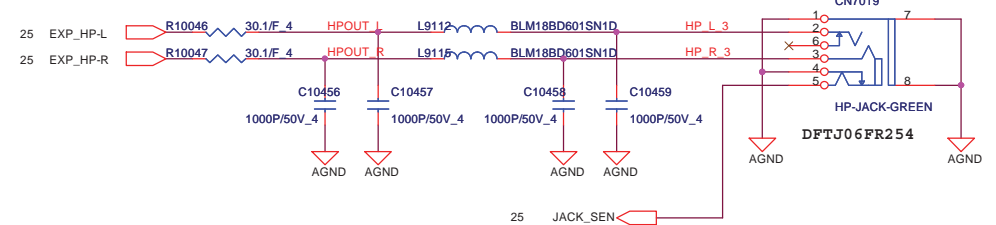
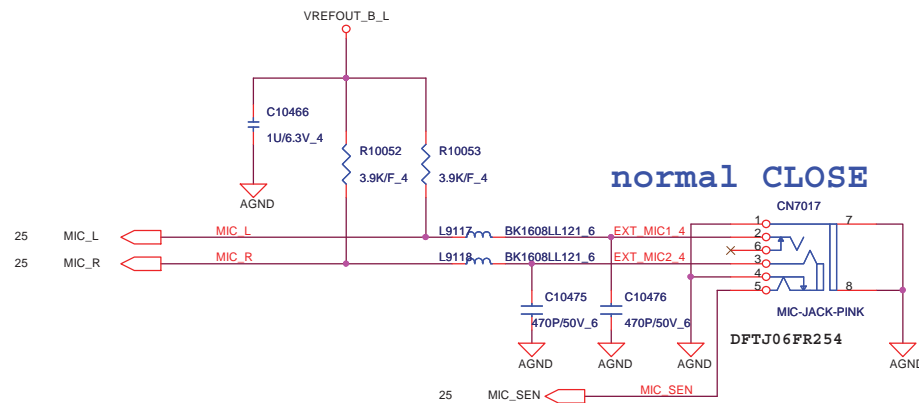
Size	Document Number	Rev
Custom	Park_MEM_Interface	2B
Date:	Tuesday, December 15, 2009	Sheet 21 of 43





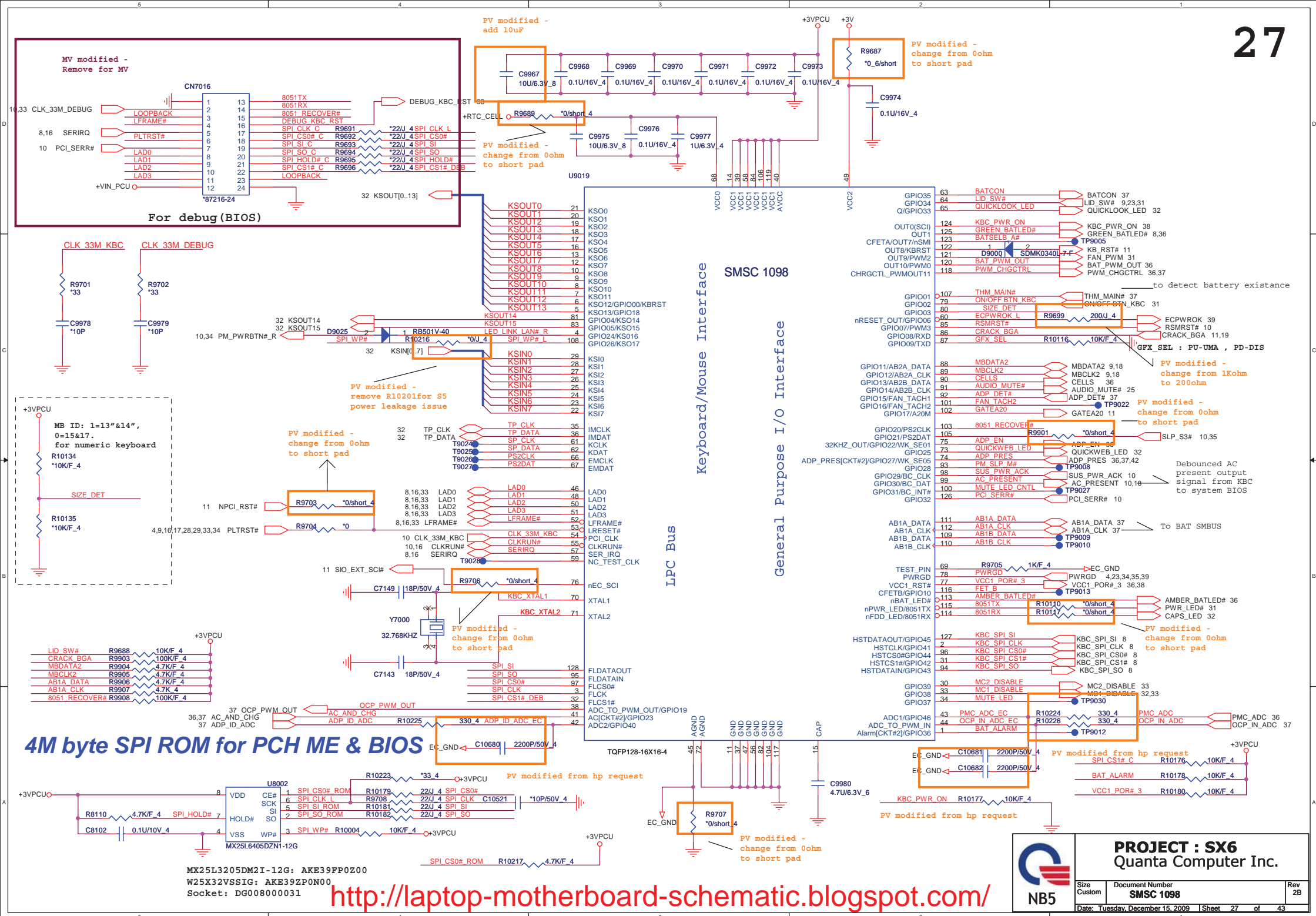


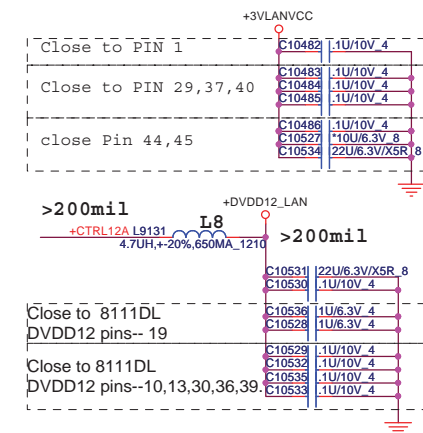


INT. SPEAKER**Headphone Jack****normal CLOSE****EXT Mic Jack****normal CLOSE**

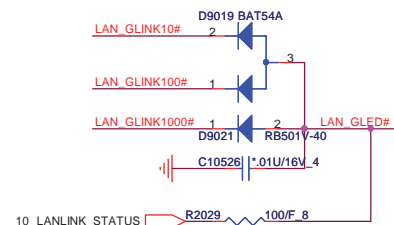
Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.





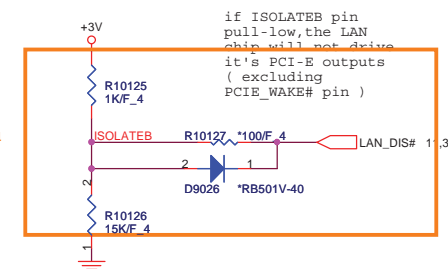
PV modified
- change
from 0ohm to
short pad



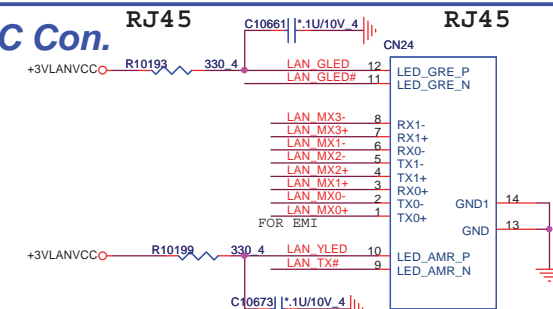
```

R461 and R463 are used in
RTL8111DL , remove R463 if
switching regulator is enable
, Remove R461 external power
is used.

```



Lan and MDC Con.



PV modified footprint

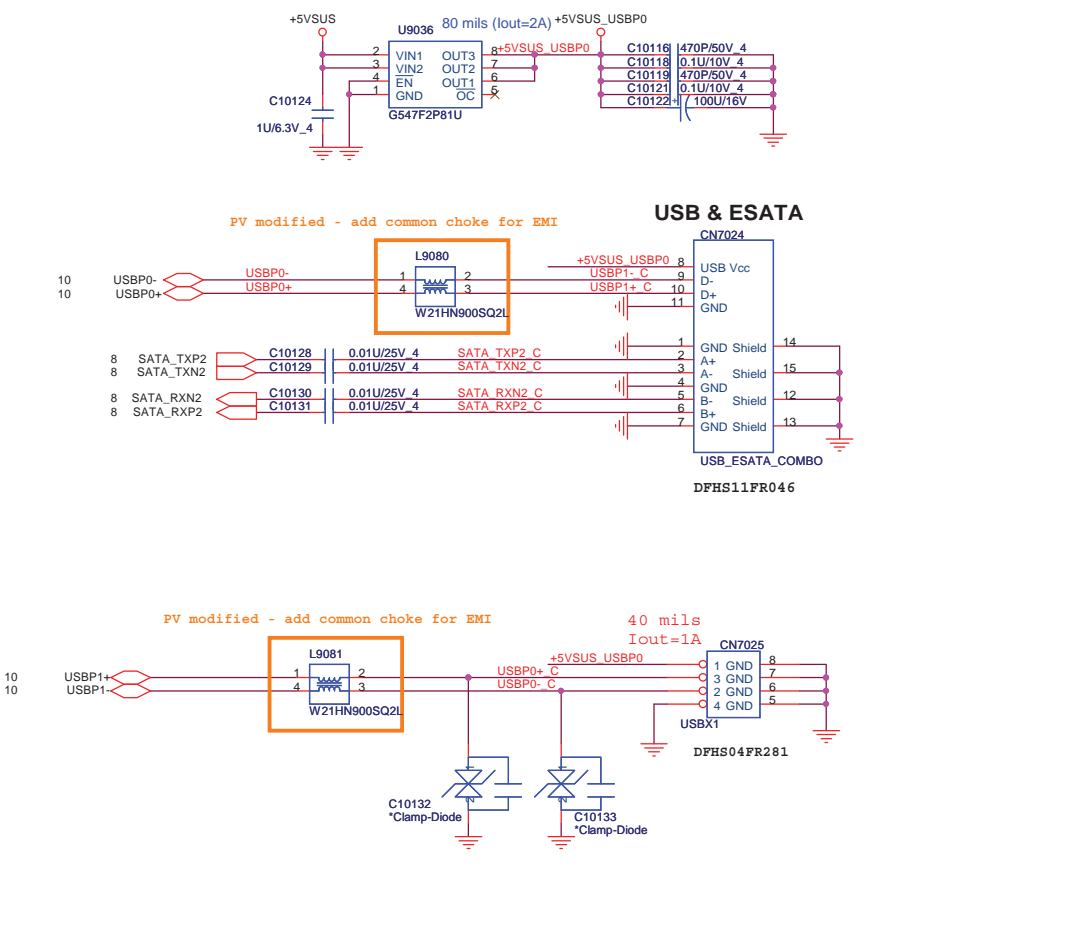
<http://laptop-motherboard-schematic.blogspot.com/>



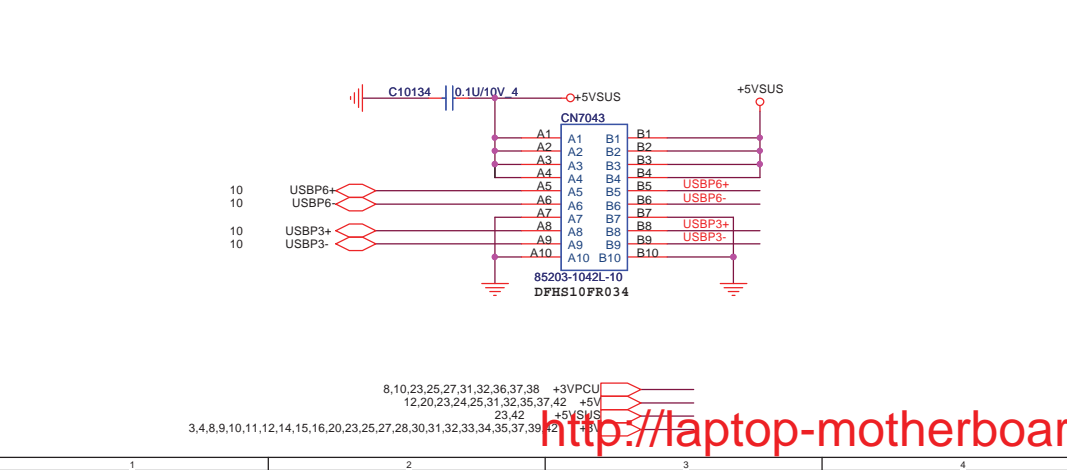
PROJECT : SX6
Quanta Computer Inc.

Size Custom	Document Number RTL8151DH-GR	Rev 2B
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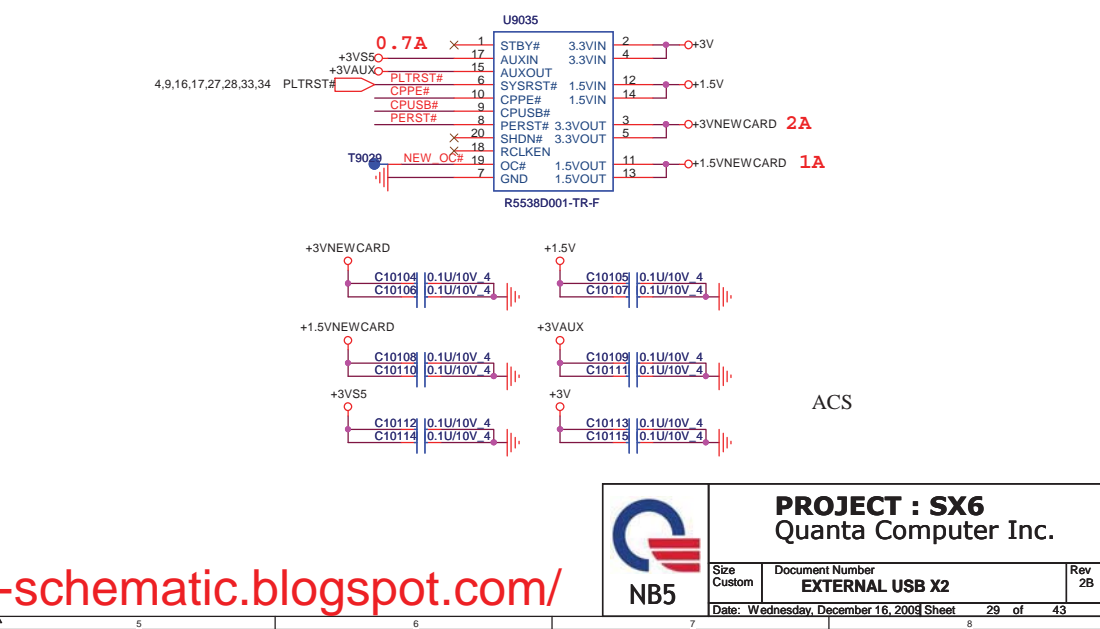
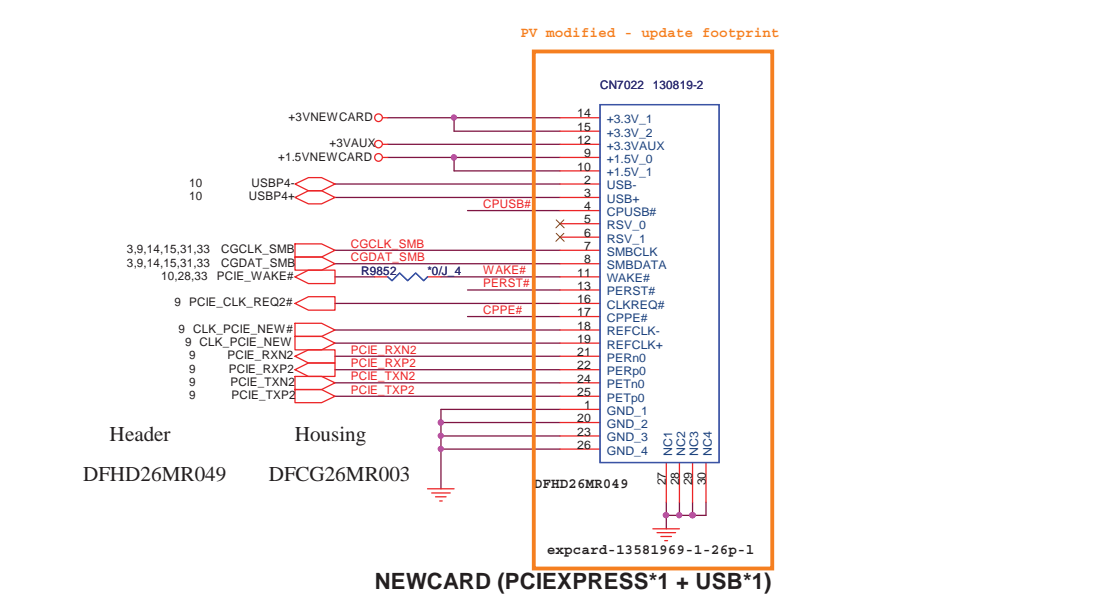
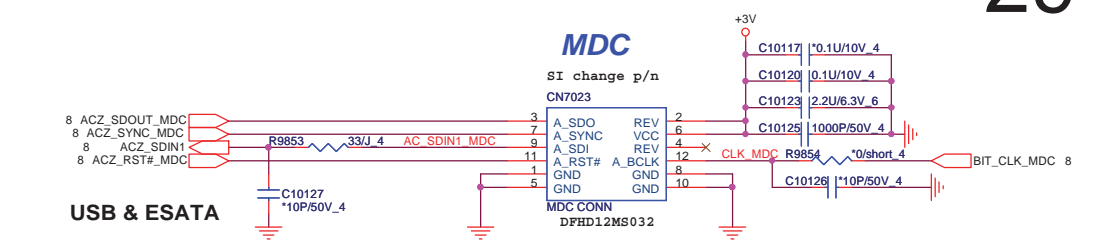
LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2

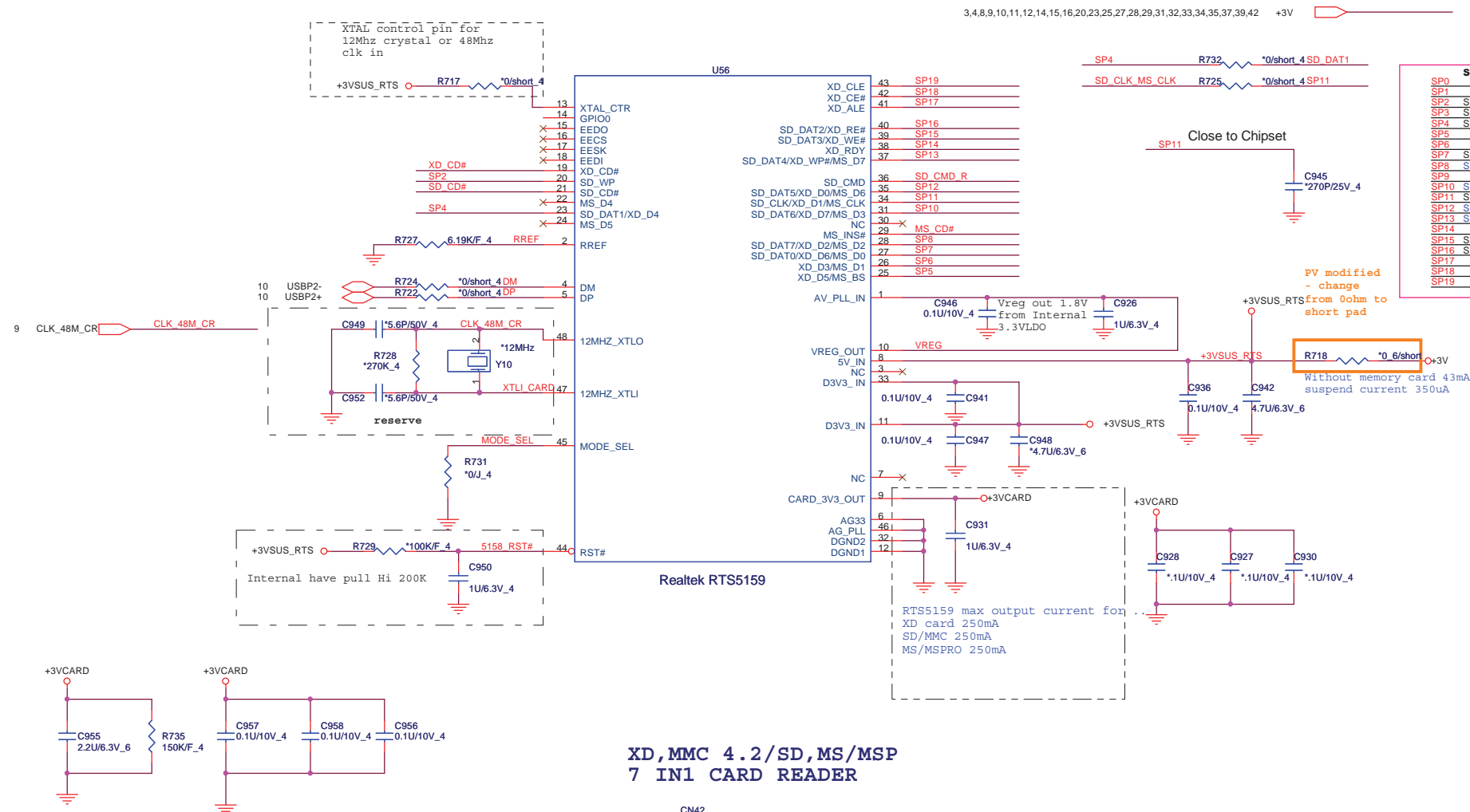


Modem CONN

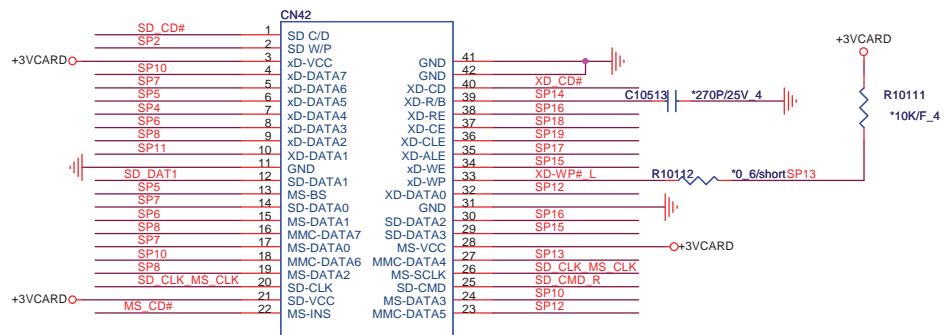


Note:


SP0	SD/MMC 4.2	MS	XD
SP1	SD WP		XD CD#
SP2	SD CD#		
SP3	SD DAT1		XD D4
SP4	SD DAT0	MS BS	XD D5
SP5		MS D1	XD D3
SP6	SD DAT7/MMC DAT7	MS D2	XD D2
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT6/MMC DAT6	MS D3	XD D7
SP9	SD DAT5/MMC DAT5	MS SCLK	XD D1
SP10	SD DAT4/MMC DAT4		XD D0
SP11			XD WP#
SP12			XD R/#
SP13			XD WE#
SP14			XD RE#
SP15			XD ALE
SP16			XD CE#
SP17			
SP18			
SP19			



**XD, MMC 4.2 /SD, MS/MSP
7 IN1 CARD READER**



PLASTREN CM7S-02 CARD READER SOCKET
DFHD42MR011



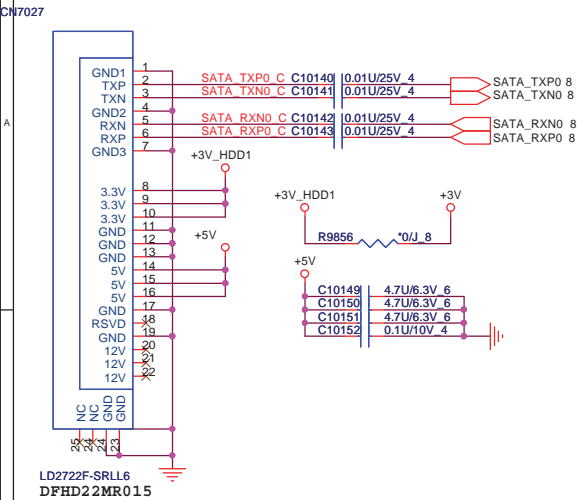
PROJECT : SX6
Quanta Computer Inc.

Size Custom Document Number
RTS5159 & CR SOCKET

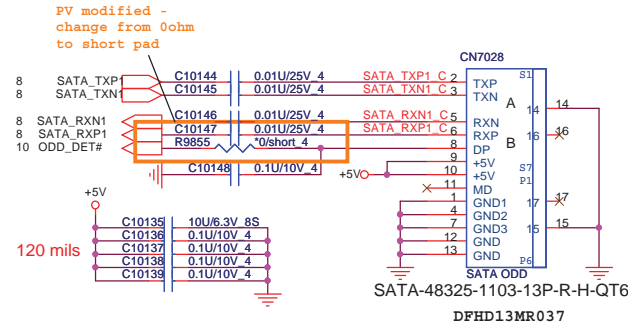
Date: Tuesday, December 15, 2009 Sheet 30 of 43

Rev 2B

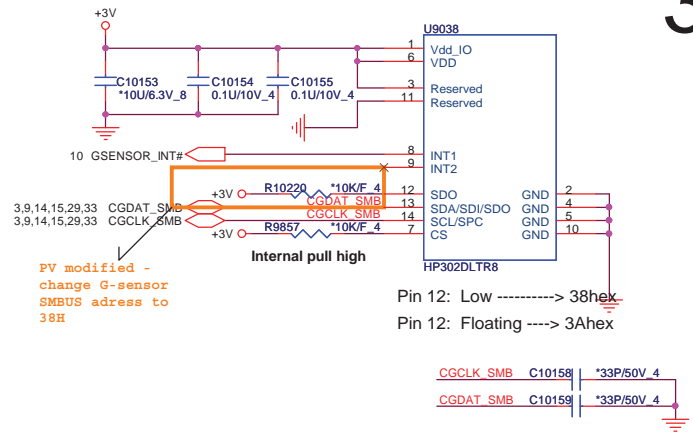
SATA HDD CONNECTOR



SATA CD-ROM

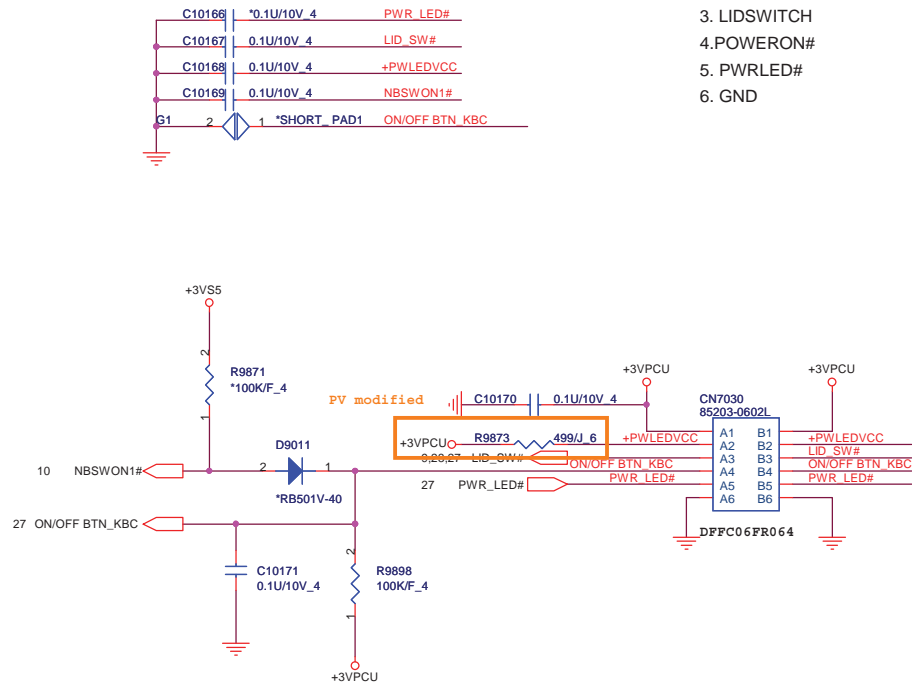


Accelerometer Sensor

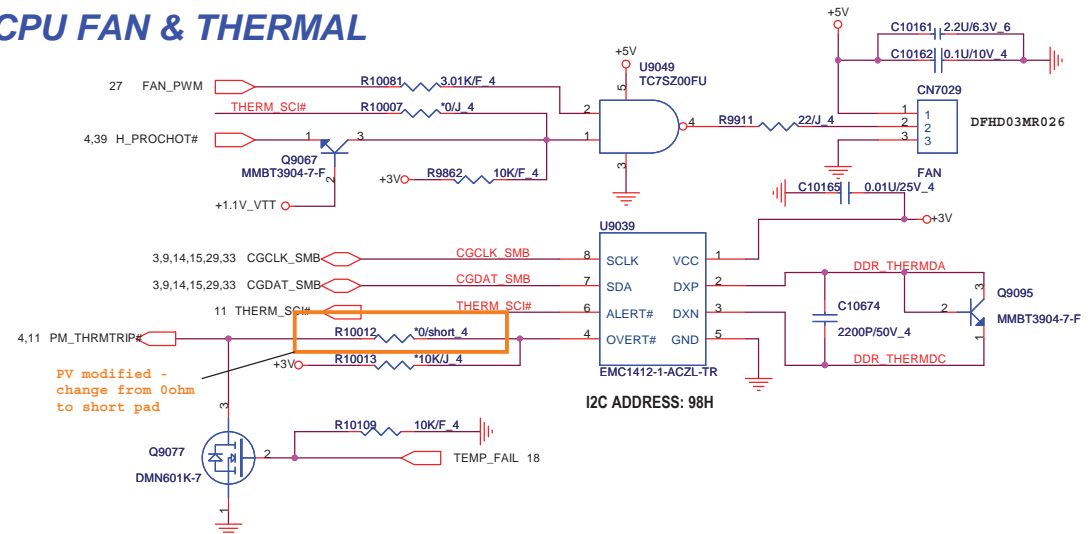


POWER BOTTON CONNECT

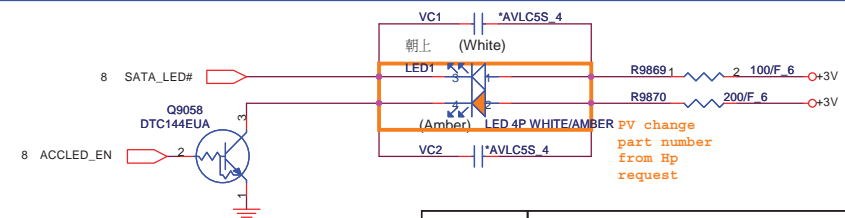
- 1.+3VPCU(LIDSWITCH PWR)
- 2.LEDVCC(+3VPCU)
- 3.LIDSWITCH
- 4.POWERON#
- 5.PWRLED#
- 6.GND



CPU FAN & THERMAL

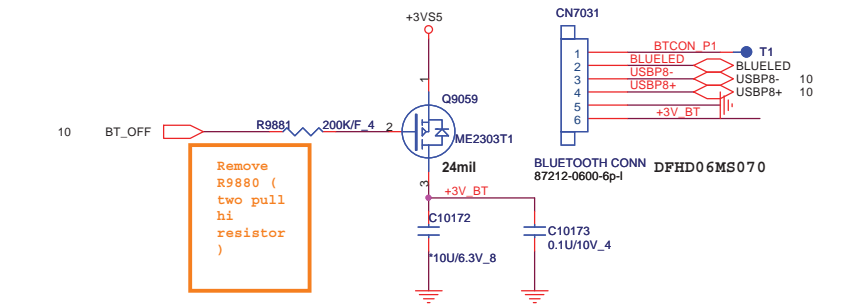


LED

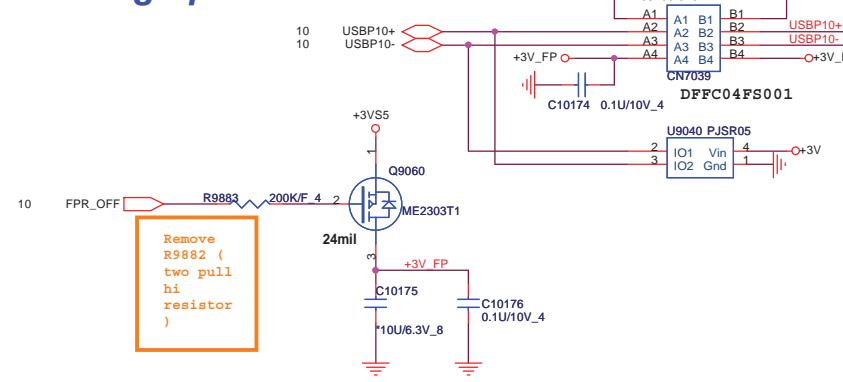


For PA 9,10,11,12,14,15,16,20,23,25,27,28,29,30,32,33,34,35,37,39,42 +3V
8,10,23,25,27,32,36,37,38 +3VPCU
4,9,10,11,12,29,32,33,34,38,41,42,43 +3VSS

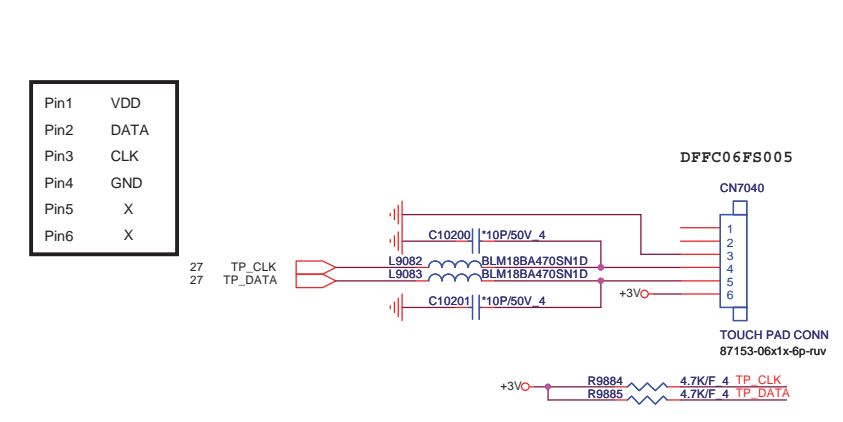
BLUETOOTH



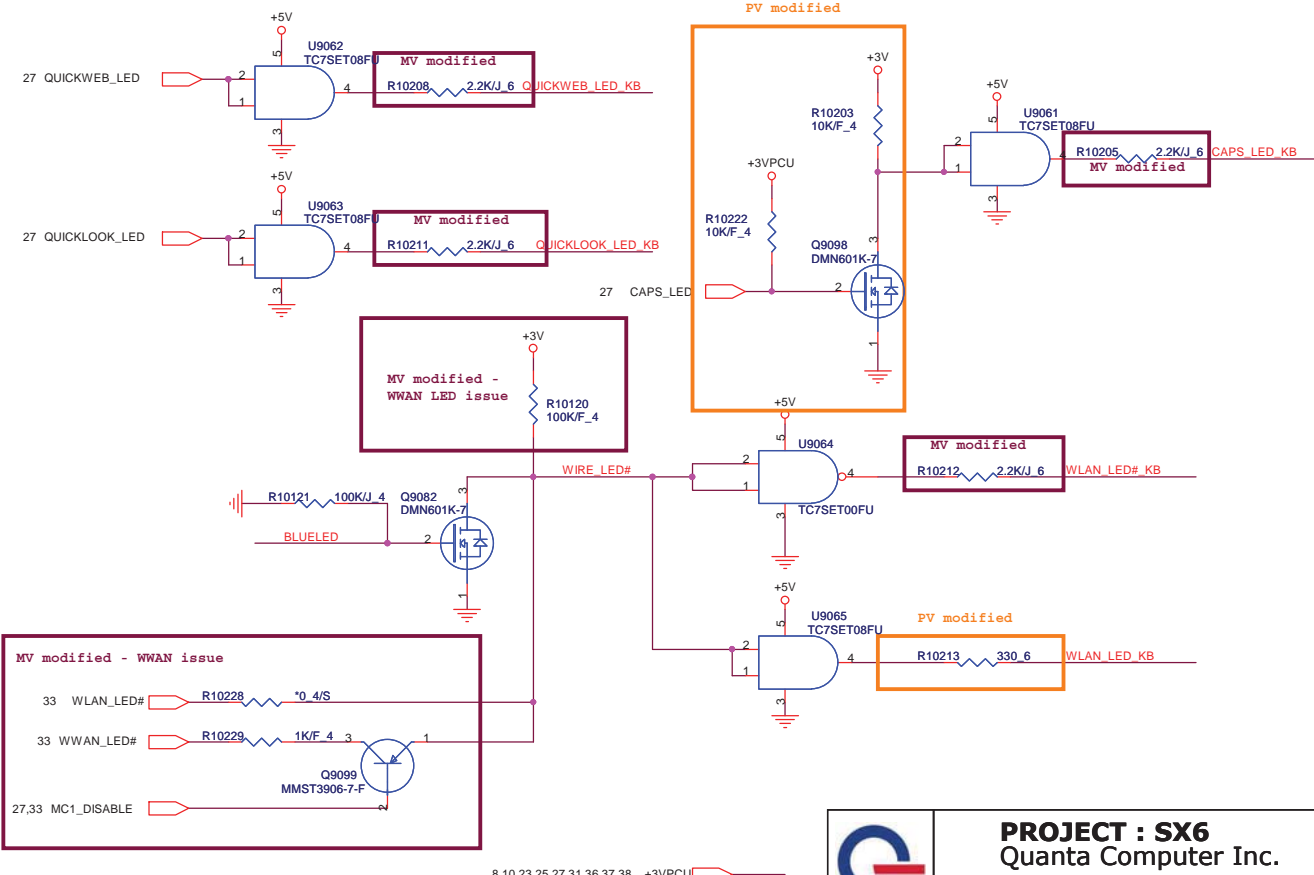
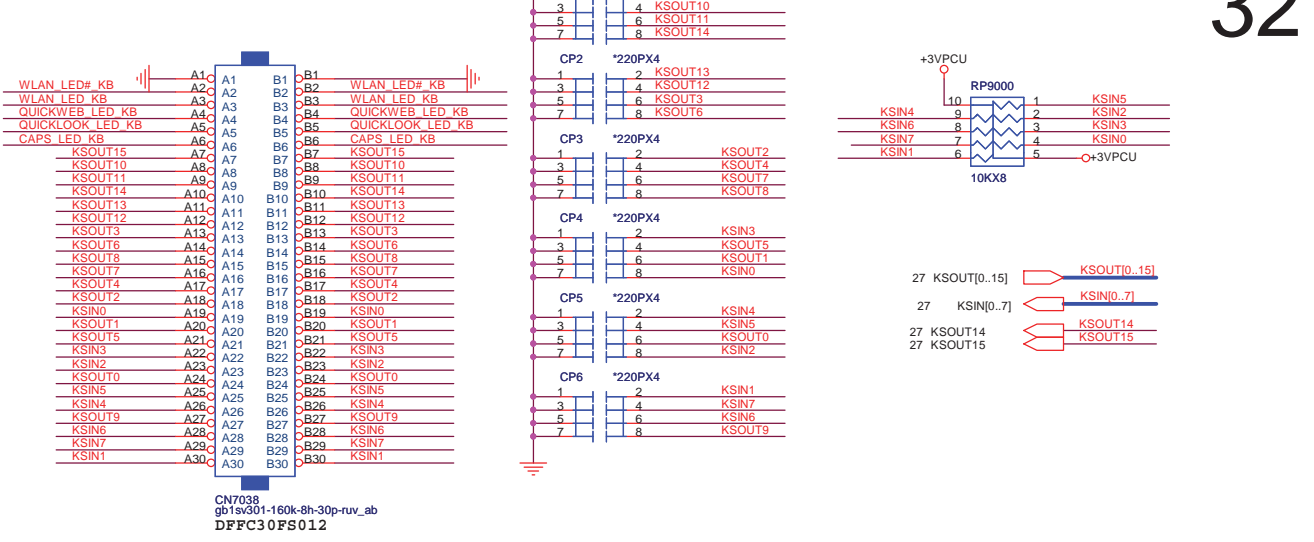
USB fingerprint CON



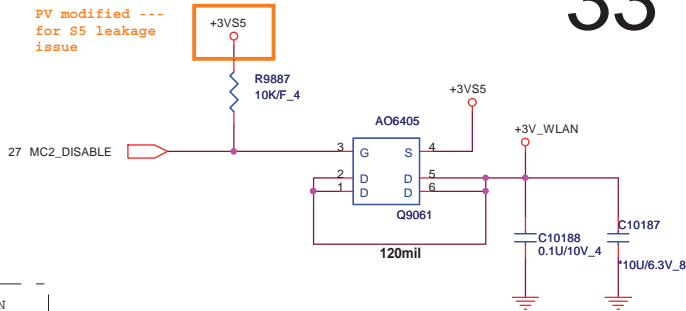
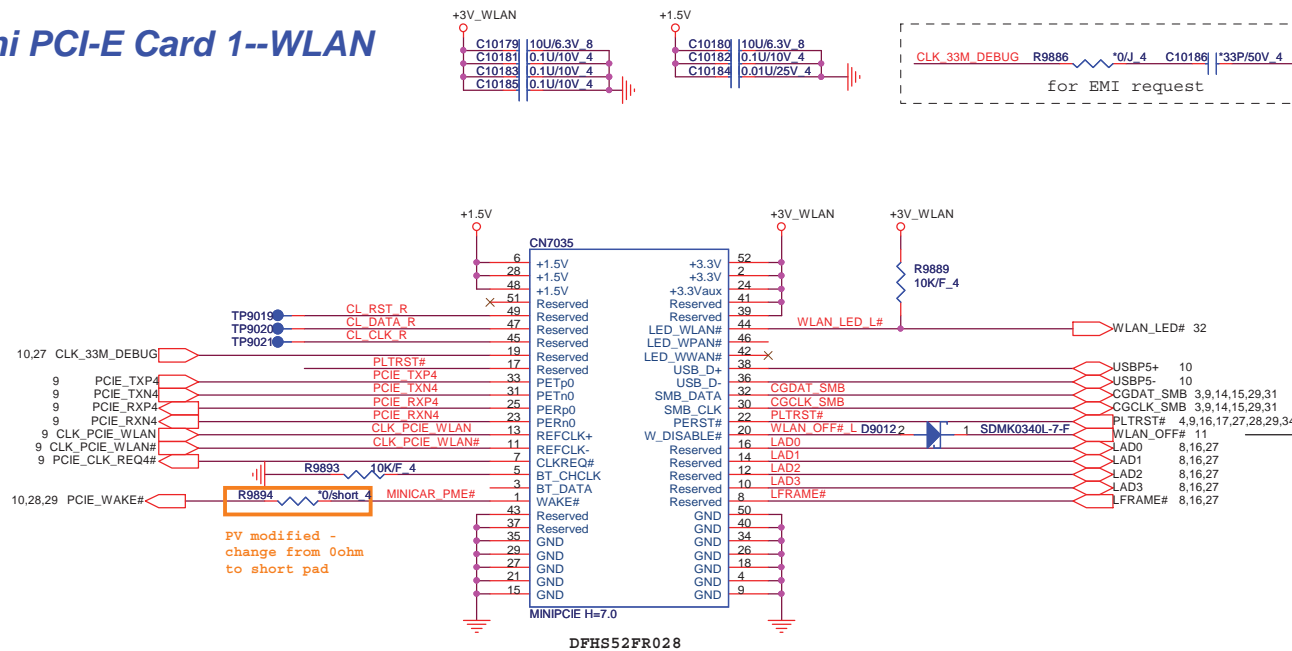
TOUCH PAD CONNECTOR



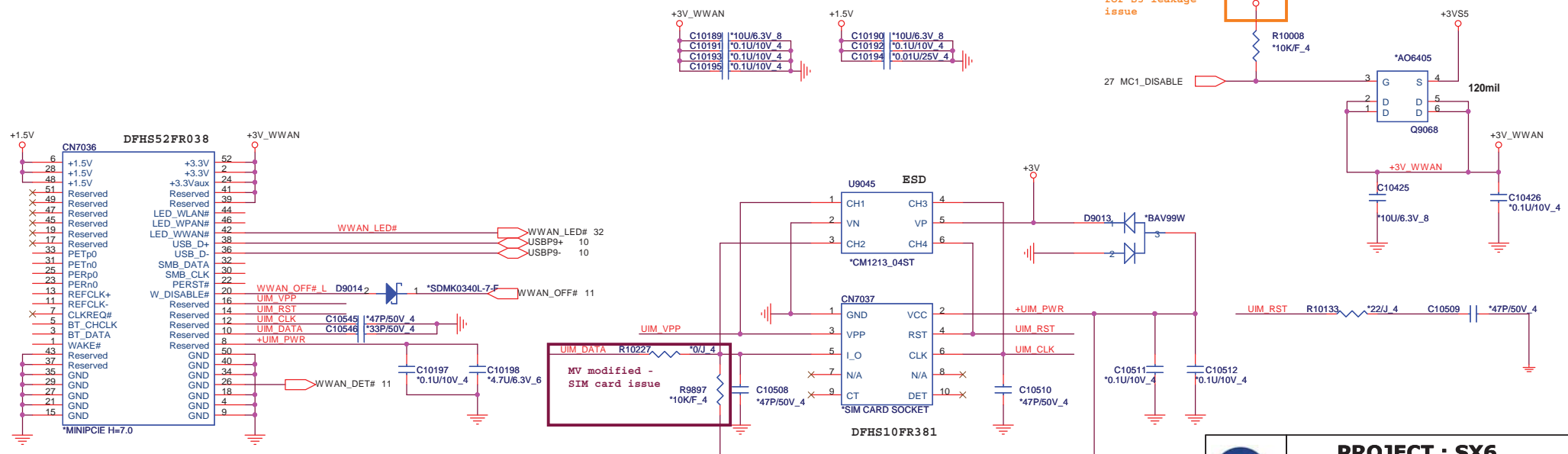
KEYBOARD CONNECTOR.



Mini PCI-E Card 1--WLAN

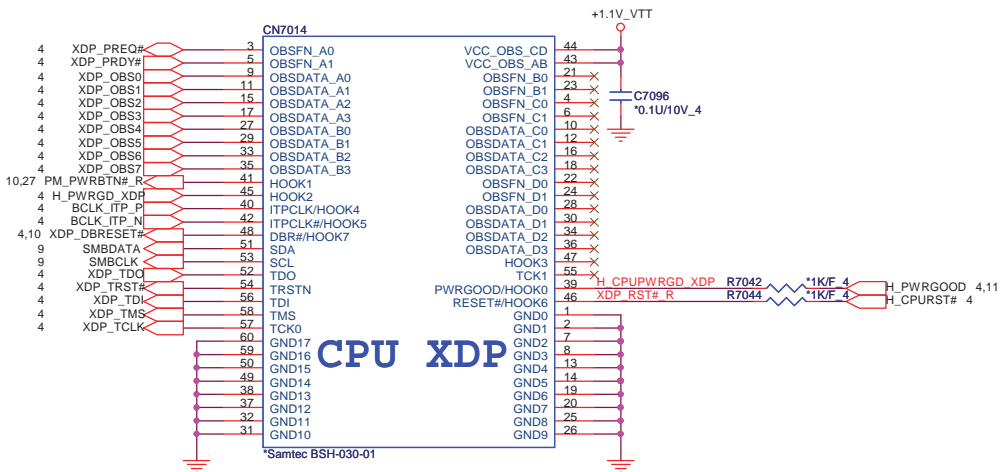


Mini PCI-E Card 2 --WWAN

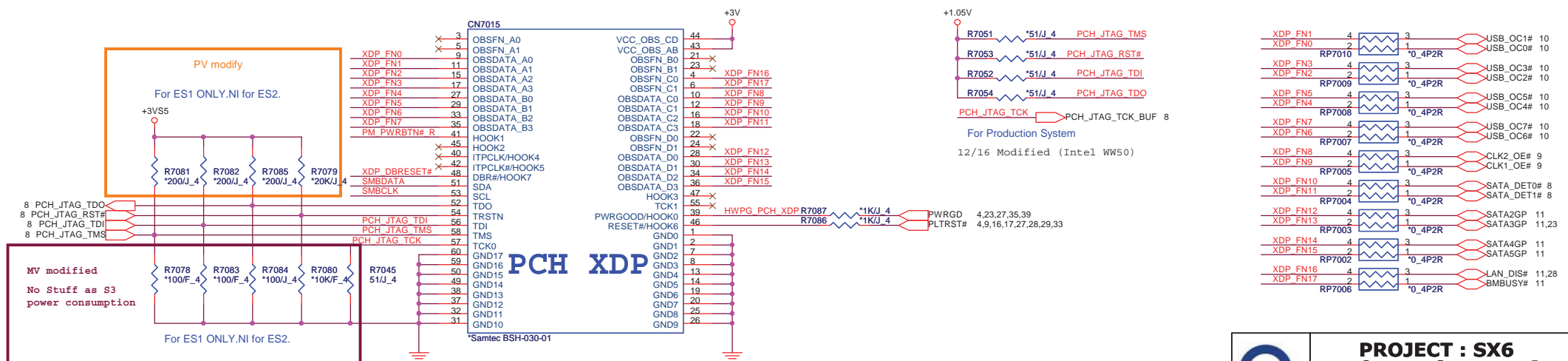
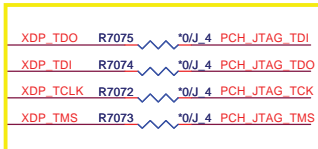


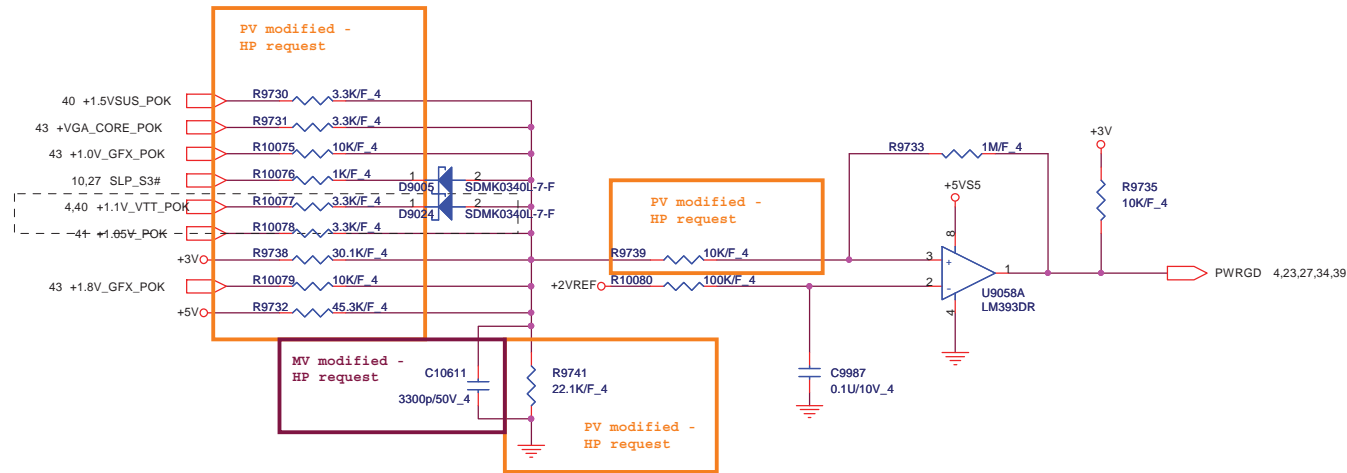
PROJECT : SX6
Quanta Computer Inc.

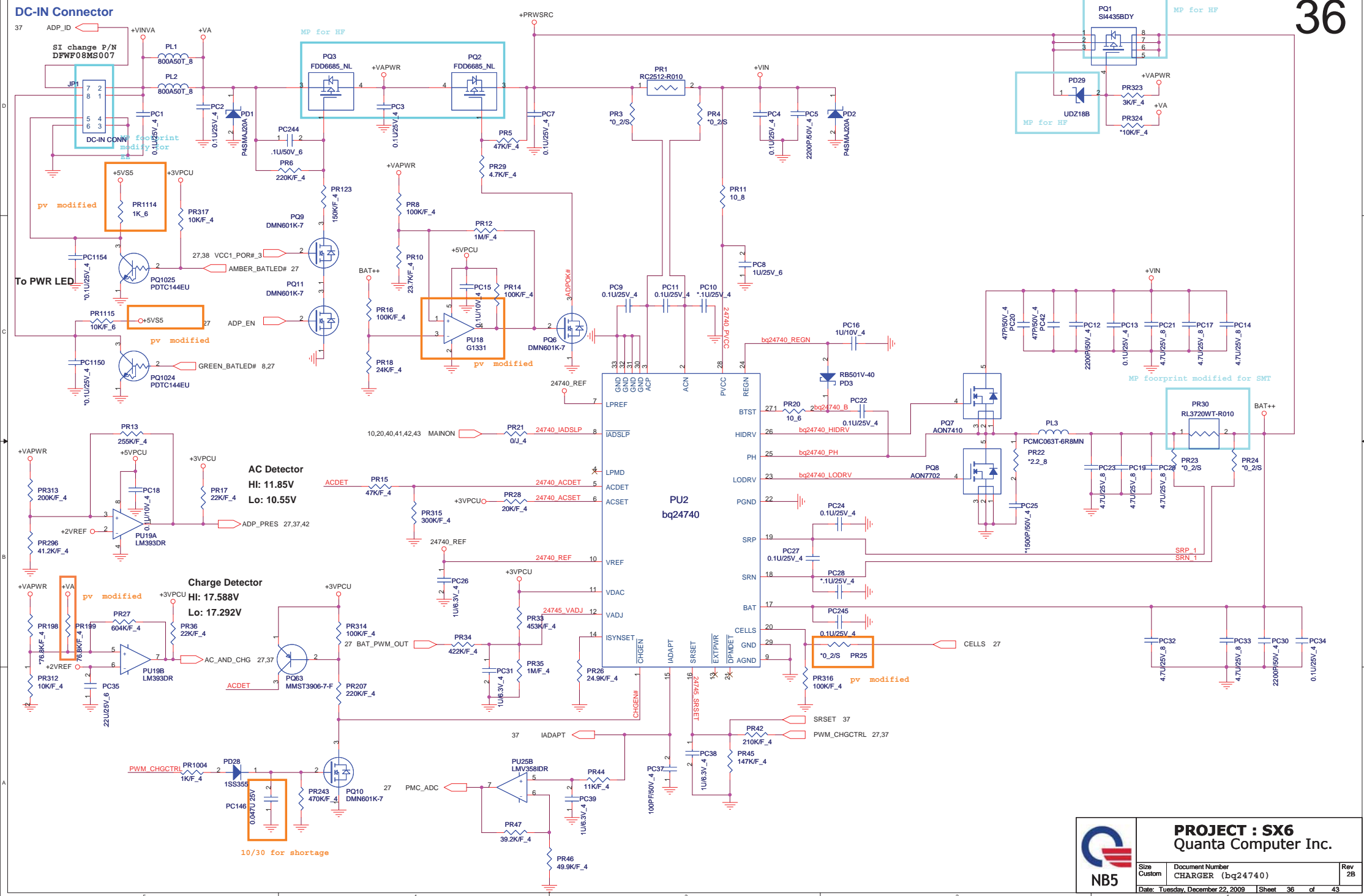
Size	Document Number	Rev
Custom	MINI PCIE CONN X2	2B
Date: Tuesday, December 15, 2009	Sheet 33 of 43	

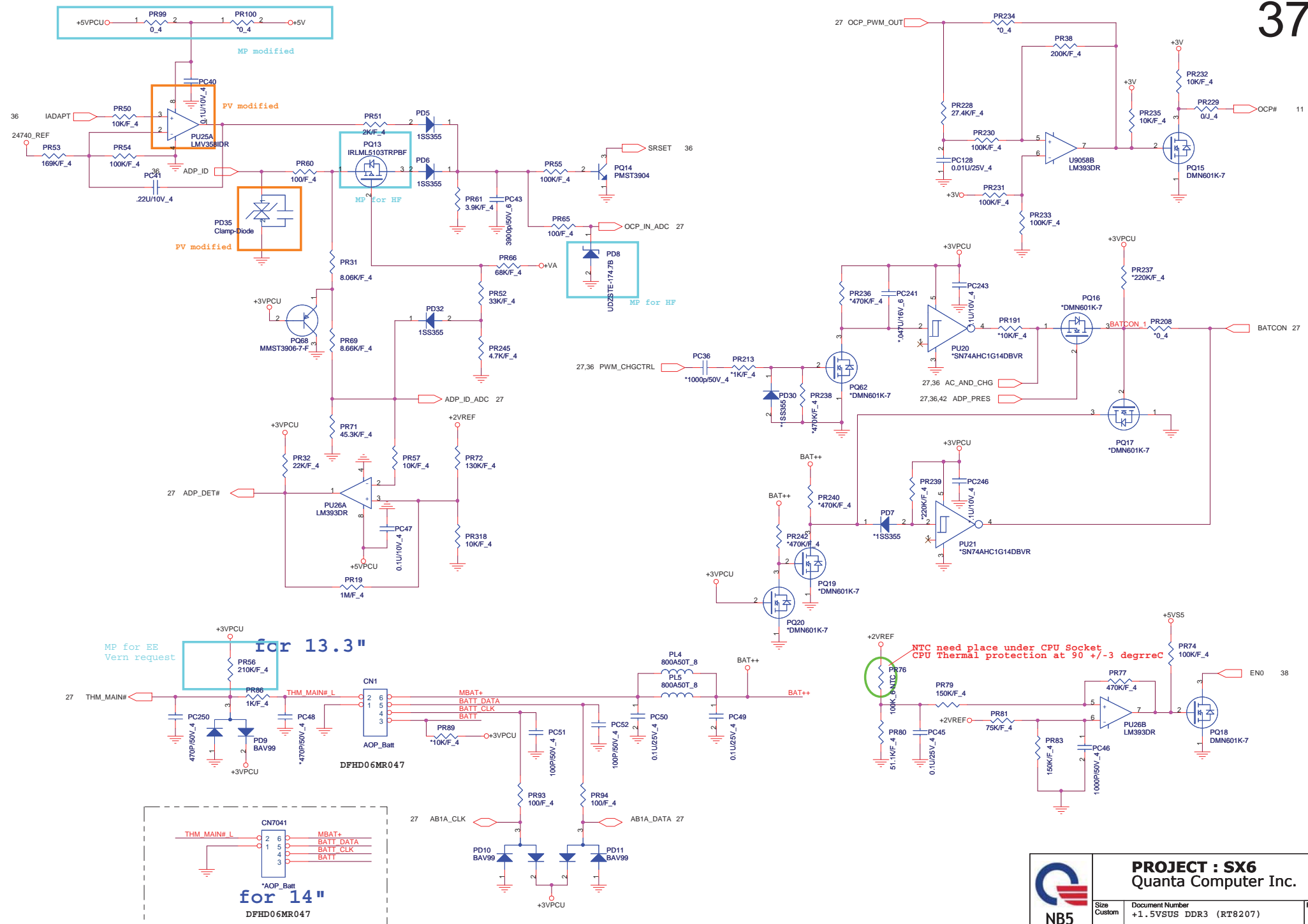


Reserve for BSDL


<http://laptop-motherboard-schematic.blogspot.com/>





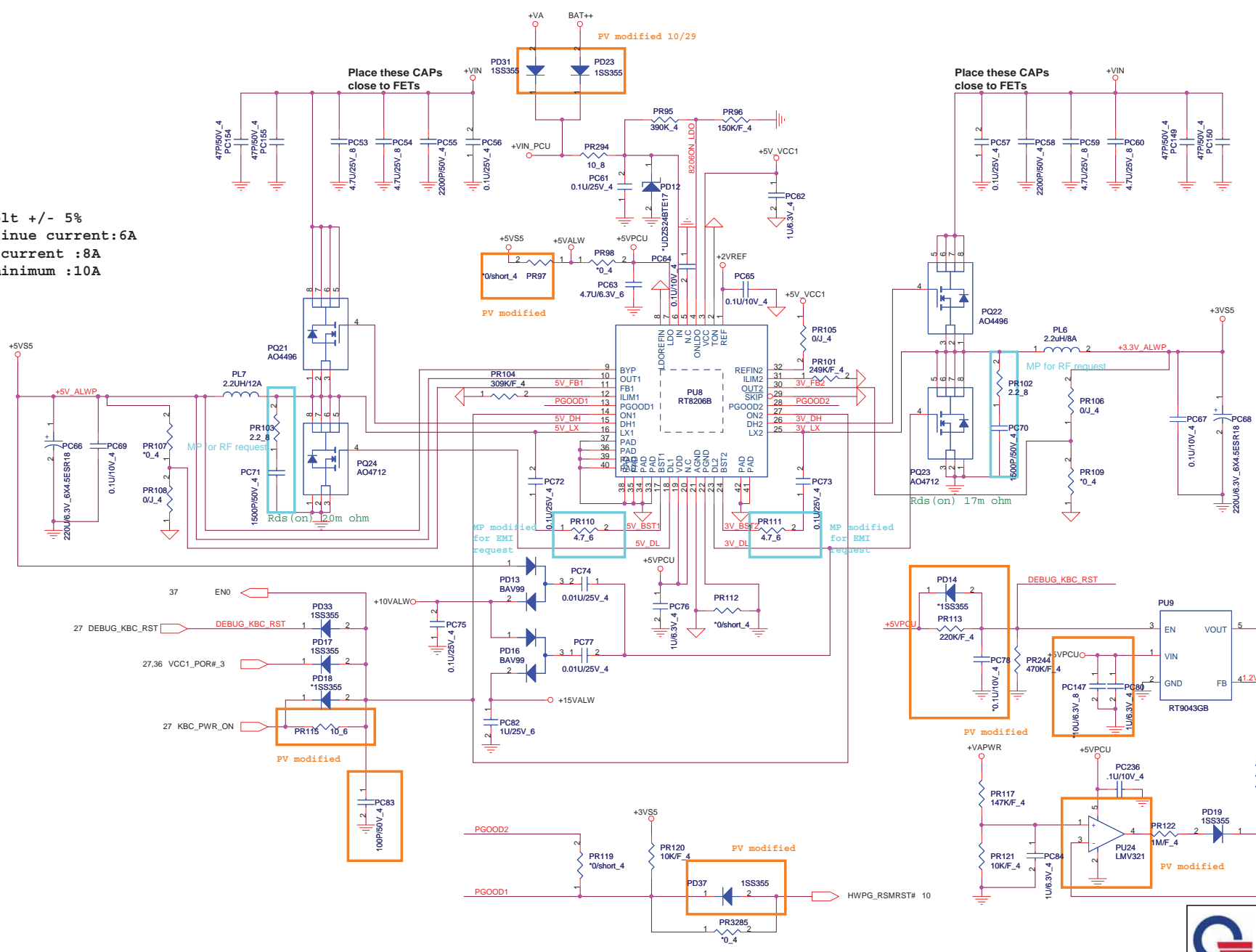


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5 Volt +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

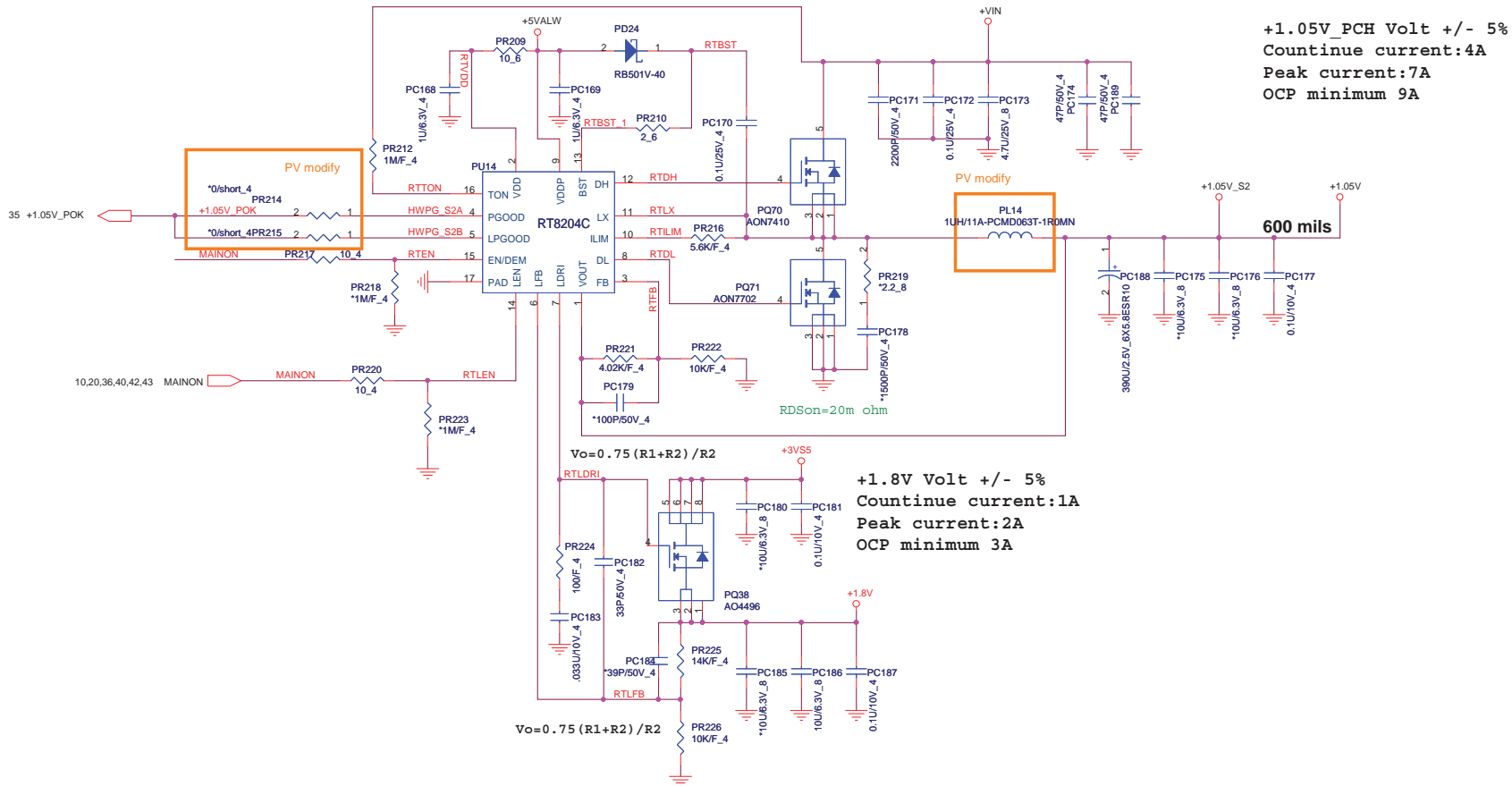
+3.3 Volt +/- 5%
Countinue current: 100mA



PROJECT : SX6
Quanta Computer Inc.

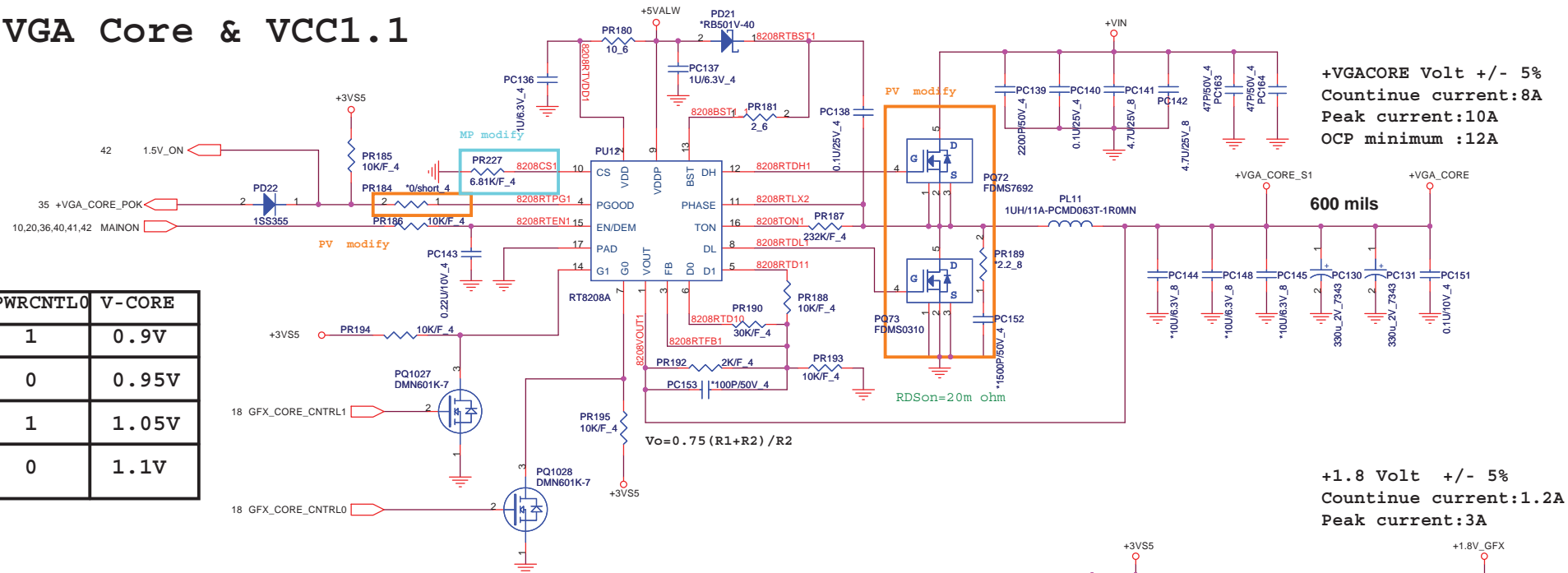
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 2B
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VGA Core & VCC1.1



	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

